

FABRICATION AND EVALUATION OF InSb CID ARRAYS

FINAL REPORT

Contract No. N00014-75-C-0124

**Prepared by:
J. C. Kim**

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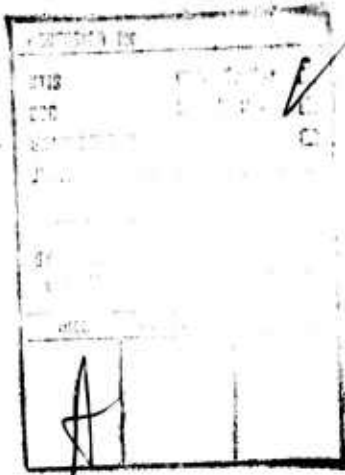
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using a multi-layer metallization process. An overlapping structure was used to obtain charge transfer between the row and column gates in each resolution element. These arrays are then mated with silicon MOS scanners on a common substrate, operating as a focal plane array. The two-dimensional mode of operation has been demonstrated for these arrays, thus making area arrays feasible.

InSb CID linear arrays are highly sensitive. All the noise sources of the devices have been identified and the measured results compare favorably with theoretical values; the number of noise carriers for the amplifier is about 100 and for the dark current it is approximately 140. Thus, for background photon flux levels higher than mid- 10^{12} photons/sec-cm², the device performance is practically background limited (BLIP).



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General Electric Company
Optoelectronic Systems Operation
Electronic Systems Division
Syracuse, New York 13201

FOREWORD

This Final Technical Report was prepared by the Optoelectronic Systems Operation of the Electronic Systems Division, General Electric Company, Syracuse, New York under Contract No. N00014-75-C-0124, entitled "Fabrication and Evaluation of InSb CID Arrays".

The work was sponsored by Naval Electronic Systems Command and Defense Advanced Research Projects Agency and administered under the direction of the Naval Research Laboratory. Dr. W. D. Baker was the Project Monitor at NRL.

Mr. J. M. Hooker, Manager of Engineering, was the Program Administrator. Dr. J. C. Kim was the Principal Investigator, directing the overall program. The array process work was performed by W. E. Davern, T. Shepelavy and V. F. Meikleham. Mr. D. Colangelo was responsible for the circuits used for device evaluation and Mr. M. D. Gibbons was responsible for the design of silicon shift register scanners.

The work was performed for the period of September 1974 through September 1975.

ABSTRACT

The InSb MIS technology has progressed to the point where high-sensitivity InSb CID line arrays and 1×16 single column arrays configured in a form identical with that required for one line of an area array, have been successfully fabricated. Also, the interface properties of the InSb-SiON MIS system have been improved and surface state densities as low as $\text{mid-}10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ have been obtained.

InSb CID 1×16 single-column two-dimensional arrays have been fabricated using a multi-layer metallization process. An overlapping structure was used to obtain charge transfer between the row and column gates in each resolution element. These arrays are then mated with silicon MOS scanners on a common substrate, operating as a focal plane array. The two-dimensional mode of operation has been demonstrated for these arrays, thus making area arrays feasible.

InSb CID linear arrays are highly sensitive. All the noise sources of the devices have been identified and the measured results compare favorably with theoretical values; the number of noise carriers for the amplifier is about 100 and for the dark current it is approximately 140. Thus, for background photon flux levels higher than $\text{mid-}10^{12} \text{ photons/sec-cm}^2$, the device performance is practically background limited (BLIP).

TABLE OF CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page No.</u>
I	Introduction	1
II	Material Preparation	5
III	Interface State Density of InSb MIS Structures .	9
IV	Measurements of High Sensitivity InSb CID Linear Array	25
	1. Measurement Setup	25
	2. Noise Sources of the System	28
	3. Transfer Characteristic	30
	4. Background Limited Performance	33
V	Fabrication of InSb CID Array	38
	1. Array Mask Design	38
	2. InSb CID Array Fabrication	40
	3. Array Package and Interconnection	48
VI	Silicon Scanner Design, Fabrication and Operation	51
	1. Introduction	51
	2. Circuit Description	52
	3. Scanner Operation	54
	4. 16-Stage Scanner	57
VII	Array Evaluation and Measurements	66
	1. Measurement Setup	66
	2. Array Test Circuits	70
	3. Array Measurements	77
VIII	Conclusions and Recommendations	83
References	85

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page No.</u>
1	Surface State Density Versus Time of InSb MIS Technology Development, Representing the Technology Progress	2
2	Proposed Series-Parallel Scan InSb CID Focal Plane Array	3
3	Steady State Maximum Depletion Width of InSb MIS Structure versus Impurity Concentration	7
4	C-V Data Measured in Poor Vacuum Right After Device Fabrication	10
5	C-V Data After Baking at 100°C for About 120 Hours in High Vacuum	11
6	C-V Data After Exposure to Air and Re-Baking at 100°C for About 70 Hours in High Vacuum.	12
7	C-V Data Re-Measured After Storing in the Same Vacuum for Three Months	13
8	C-V Data of a Line Array After Baking at 105°C for Six Days in High Vacuum	14
9	C-V Characteristics of InSb MIS Structure After High Vacuum Bake-Out	16
10	G/ω_m - Voltage Characteristics of InSb MIS Structure	17
11	Simplified Equivalent Circuit for an MIS Structure Showing the Interface State Branch	18
12	Parallel Representation of C_s and R_s of the Equivalent Circuit shown in Figure 11	18
13	Surface State Density (N_{ss}) Versus Surface Potential (ϕ_s)	22
14	Surface State Time Constant Versus Surface Potential	24
15	Experimental Setup Used in the Sensitivity Measurements of InSb CID Line Array	26
16	Equivalent Circuit for the Enable-Line Readout Used in the Measurement Setup Shown in Figure 15	29

List of Illustrations Contd.

<u>Figure</u>		<u>Page No.</u>
17	Operating Pulse Waveforms Used in the Measurement Setup Shown in Figure 15	29
18	Transmission Curve of a 4.18 μm Spectral Filter Used in the Sensitivity Measurements	31
19	Transfer Characteristic of InSb CID Line Array . . .	32
20	Measured Background Shot Noise Versus the Carriers Generated by the Background Photon Flux	36
21	Design of 1x16 InSb CID Array for One-Column Area Array, Showing 16 Row Elements with Alternate Bonding Pads	39
22	C-V Characteristics of Long Lead Pattern InSb MIS Structures	42
23	C-V Data for 1x16 InSb CID Array with Thin-Field Oxide	44
24	C-V Data for 1x16 InSb CID Array Having Thick-Field Oxide	45
25	Photograph of Completely Processed 1x16 InSb CID Array	47
26	Photograph of Packaged 1x16 InSb CID Array with Two Si Scanners	49
27	Scanner Circuit Diagram	53
28	Scanner Timing Diagram	56
29	Layout of 16-Stage Silicon Scanner	58
30	Results of Simulation of the Four Stage Si Scanner. .	60
31	Photograph of 16-Stage Si Shift Register Scanners . .	61
32	Identification of the Bonding Pads for the Scanner Shown in Figure 31	62
33	Equivalent Circuit for the Si Scanner Shown in Figure 31	63
34	Test Result of the Silicon Scanner Operation	65

List of Illustrations Contd.

<u>Figure</u>		<u>Page No.</u>
35	Block Diagram of the Array Testing System	67
36	Array Mounting Fixture Inside Dewar	68
37	Optical Array Measurement Setup Used for Modulation of a Slit Image	69
38	Timing Circuits Used to Generate Appropriate Pulse Waveforms	71
39	Bias and Driver Circuits	73
40	Appropriate Timing Diagram Used for the Array Measurements	75
41	Amplifier and Sample-Hold Circuits Used for the Video Signal Processing	76
42	Schematic Diagram of InSb CID Array (1x16) Connected with Si Shift Register Scanner and Preamplifier	78
43	Array, Demonstrating Two-Dimensional Mode of Operation	80
44	Operation of 1x16 Array Using a Blackbody Source . . .	81

I. INTRODUCTION

The successful development of InSb charge injection device (CID) arrays has been made possible by the recent success of our InSb MIS technology, which is now capable of producing two-dimensional InSb CID arrays.

For the last few years, we have been involved in the InSb MIS technology^(1,2) with the goal of developing InSb charge injection devices for infrared applications. Considerable progress has been made in this new technological area, as illustrated in Figure 1. We plot here the measured interface state densities as a function of development time. It is interesting that the progress appears to be exponential time, indicating a rapid technological advance. Surface state densities of mid- $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ have been obtained.

Because of this rapid advance in the InSb MIS technology, we intend to develop two-dimensional InSb CID arrays. There is particular interest in these arrays due to their application in mechanically scanned series-parallel focal plane configurations using time delay and integration (TDI)⁽³⁾. Such a focal plane array is shown in Figure 2⁽³⁾. The InSb CID array module consists of 16x25 elements, a module of 400 sensors. The integrated information signal must be read out in series through a common preamplifier; then it is demultiplexed and inserted into 25 parallel Si CCD registers for TDI signal processing. Thus the signal must be processed from the series readout of the InSb CID module to parallel Si CCD TDI circuits. This means that the InSb CID array module must be capable of operating in the two-dimensional mode; thus, the array structure must be two-dimensional even though the arrays are to be used in a mechanically scanned system.

In two-dimensional CID arrays it is necessary that the charge be transferred back and forth between the row and column gates in each resolution element. The charge transfer and injection must occur on the basis of element selection. That is, for the selected element, the charge is injected to yield a signal while the charge on the unselected elements must be transferred to avoid charge injection. Therefore, the signal in the

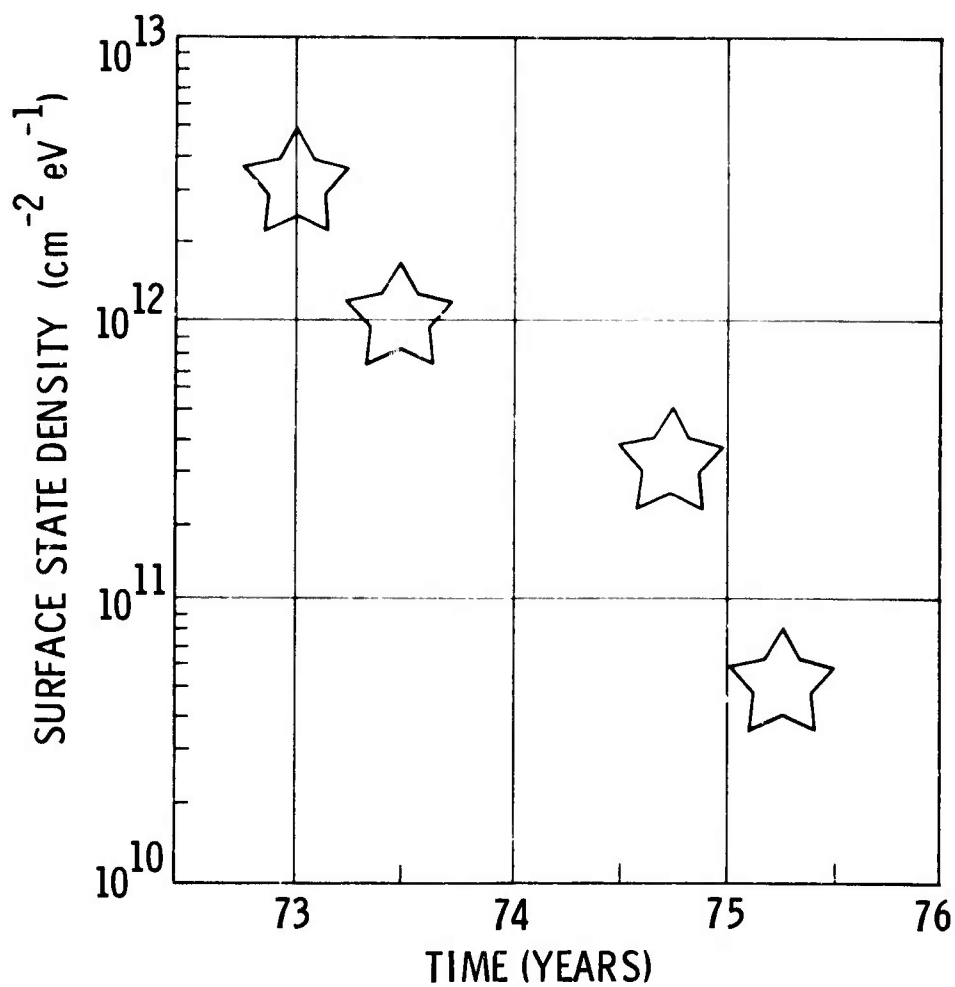


Figure 1. Surface State Density Versus Time of InSb MIS Technology Development, Representing the Technology Progress.

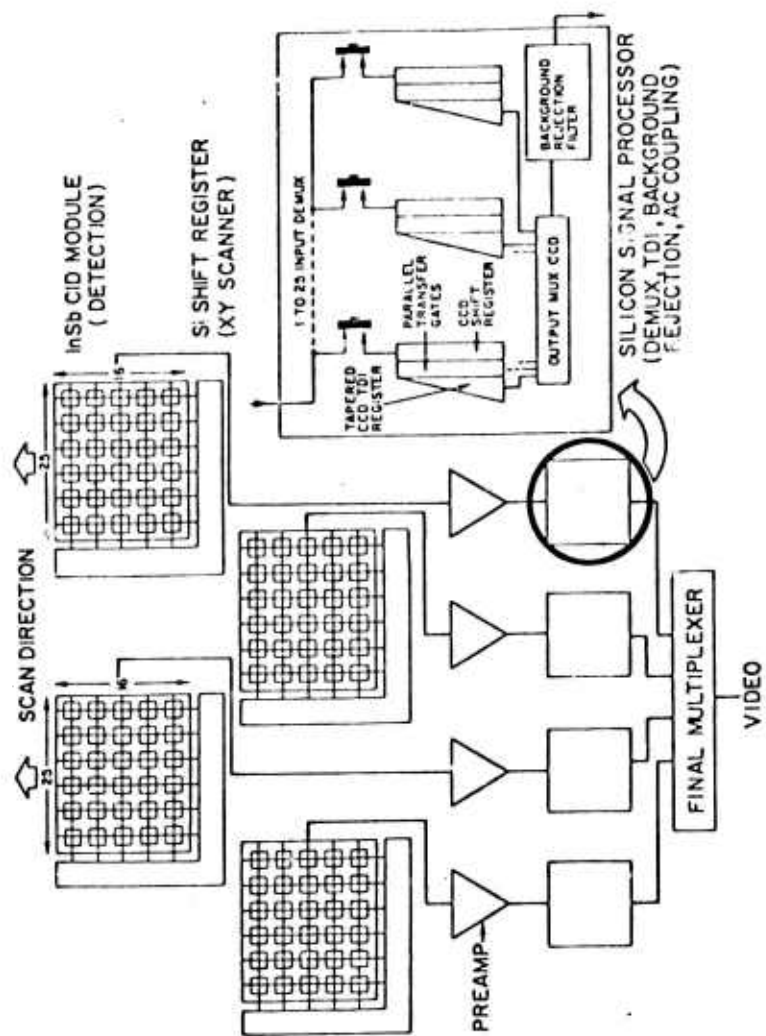


Figure 2. Proposed Series-Parallel Scan InSb CID Focal Plane Array⁽³⁾.

array can be read out sequentially through a common preamplifier by selecting one element at a time.

The objective of the present program is, however, to design, fabricate and evaluate 1x16 single column arrays; these are not linear arrays but area array structures. Sixteen stages of silicon shift register scanners will be used to scan the 16-row-elements, while the one column line is used to process the video signal. Both the InSb array and silicon scanners will be operated at the same temperature in a cryogenic dewar.

from 1 → This Final Report describes the development of 1x16 two-dimensional InSb CID arrays. The InSb wafer material preparation is described in Section ²~~II~~. The improved ³interface state densities of InSb MIS structures are presented in Section ~~III~~³. The sensitivity measurements of linear arrays is discussed and the results are presented in Section ⁴~~IV~~. In Section ⁵~~V~~, we describe the array fabrication process; silicon shift register scanners are discussed in Section ⁶~~VI~~. The array evaluation measurements are discussed in Section ⁷~~VII~~ and finally, conclusions and recommendations are presented in Section ⁸~~VIII~~.

9

II. MATERIAL PREPARATION

Single crystal Te-doped n-type InSb ingot materials with carrier concentrations in the range of mid- 10^{14} to 10^{16} carriers/cm³ were purchased. The materials were generally grown by the Czochralski method, but we have also used boat-grown crystals. The following general criteria were employed in the selection:

1. Low etch-pit dislocation density, typically less than 100 EPD/cm².
2. Uniform distribution of impurity concentration along the crystal ingot.

Before we purchase large quantities of single-crystal InSb materials, we evaluate them extensively in order to determine their suitability for CID devices. Simple MIS structures were used for the material evaluation; this work was reported in reference (4).

The crystals were sliced into wafers with a wire saw to a thickness of about 35 mils. The diameter of the wafers ranged from 2 to 3 cm. Both sides of the wafers were lapped flat and parallel, to a final thickness of about 20 mils. Then the B-face side was mechanically polished to a mirror-like surface, after which it was further polished with a 3% bromine in methanol solution to remove scratches. This chemical polish, however, results in an "orange-peel" type surface.

The polished wafers were then removed from the holders and boiled in trichloroethylene to remove the black wax, then they were stored in dry boxes for subsequent processing. Prior to the dielectric deposition, the polished wafers were again chemically etched with a 5 to 1 lactic/nitric acid solution, followed by a thorough wash in deionized water. Finally, the wafers were cleaned in a solution of HCl, rinsed in deionized water and allowed to dry in blowing nitrogen.

The water etching process was done uniformly with an etching fixture that held six wafers simultaneously. This batch etching process not only saves time but also improves surface uniformity. The technique has proved quite successful in preparation of the wafer materials for CID array fabrication.

SiON layers have been successfully used^(1,2) as a dielectric material for the InSb surface. This oxide is prepared by the pyrolytic decomposition of SiH_4 , O_2 , and NH_3 , in a nitrogen gas flow system. The deposition system is a vertical chamber in which the wafers are held on a graphite holder heated by an rf coil. The graphite holder can also be rotated at various speeds during the deposition to achieve uniform oxide layers. A proper mixture of SiH_4 , O_2 , and NH_3 is injected vertically into the chamber. The thickness of deposited oxide is monitored by noting the color during deposition. Typical deposition temperature is in the range of 200°C .

We have refined the deposition system⁽⁵⁾, including recalibration of the gas flow and adjustment to obtain the proper gas ratio. The gas flow rates currently used are $\text{SiH}_4 = 90$ cc/min, $\text{O}_2 = 12$ cc/min, $\text{NH}_3 = 4$ cc/min, and $\text{N}_2 = 3,500$ cc/min. The thickness of oxide ranges from several hundred to several thousand angstroms. As shown later, SiON layers have been used for the multi-layer metallization required in the CID array process.

Simple MIS structures were fabricated and the C-V characteristics were measured. Semi-transparent NiCr metal field plates were vacuum-deposited on the SiON layer through a mechanical mask; the diameter of the metal gate is typically 20-mils. TO-5 transistor headers were used to mount these devices for a quick evaluation; and the capacitance and conductance characteristics of these MIS structures were measured.

The C-V characteristics of the InSb MIS structures reveal the impurity concentration of the wafer materials and, thus, were studied as a function of material doping levels⁽⁴⁾. Figure 3 shows the steady-state depletion width on InSb surface as a function of the impurity concentration.

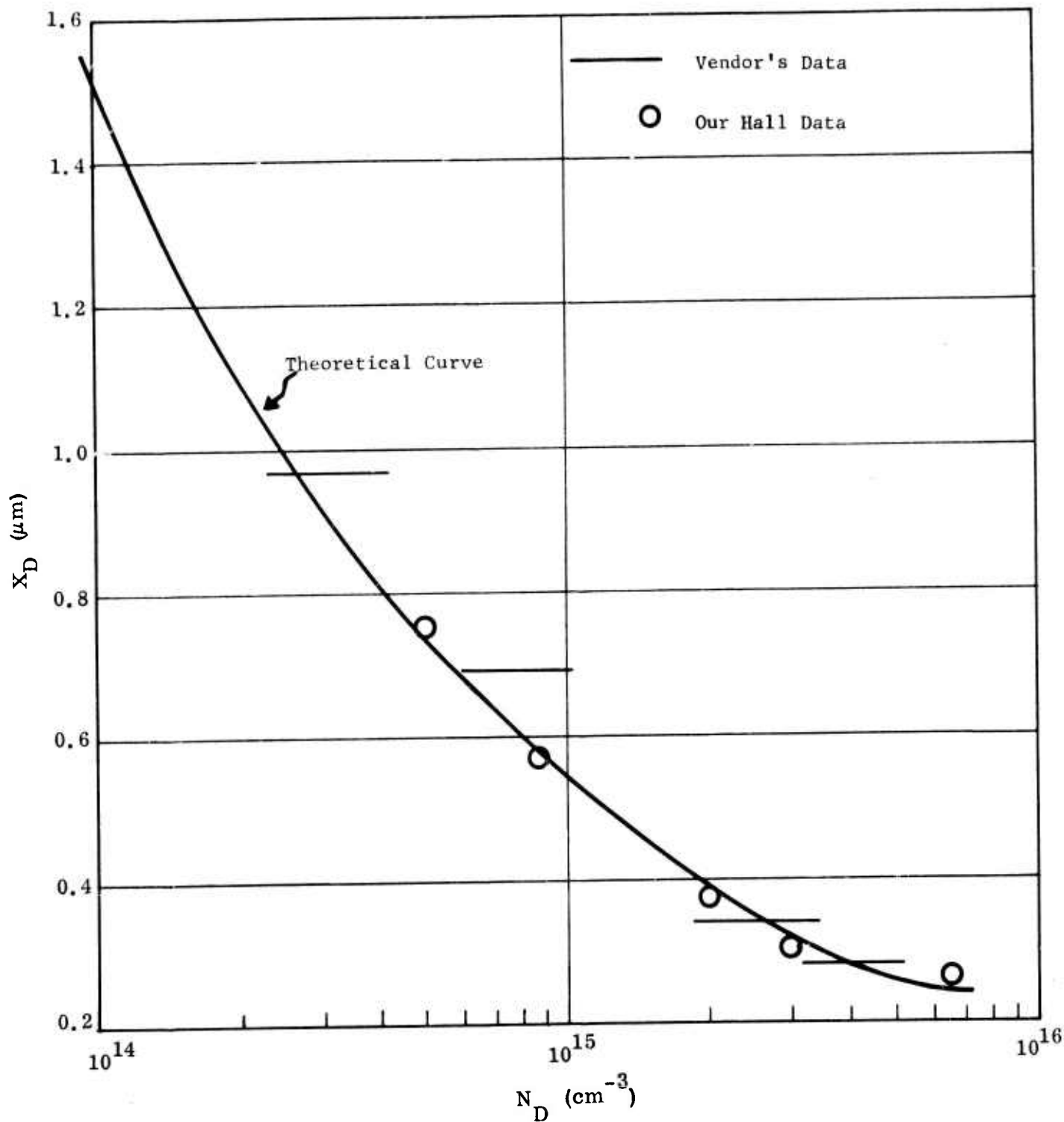


Figure 3. Steady State Maximum Depletion Width of InSb MIS Structure versus Impurity Concentration

The continuous solid line is the theoretical curve derived from the value of the depletion approximation⁽⁶⁾; the circled points represent the impurity values determined by our Hall measurements, and the short bars correspond to the impurity levels provided by the material vendors. As shown, the experimental results follow very closely the theoretical curve. The C-V data of MIS structure thus reveal the substrate doping level quite precisely and can, therefore, be used effectively for the evaluation of substrate materials.

It has been found that MIS structures with good C-V characteristics always yield excellent CID devices. We, therefore, have used the C-V data throughout this work.

III. INTERFACE STATE DENSITY OF InSb MIS STRUCTURES

Considerable improvement has been made in the interface state density of InSb MIS structures by a high-vacuum annealing process. The annealing temperature used in these experiments are typical of those encountered in the device dewar package. In order to maintain the high-vacuum integrity of the final sealed devices, the vacuum dewars are baked out and sealed off in high vacuum at relatively low temperatures. During this bakeout period, the devices in the dewar must not degrade and high-vacuum annealing shows promise for the development of good InSb CID devices.

Figure 4 shows typical C-V characteristics for a device measured in a demountable dewar with poor vacuum. Yet, the device reveals good C-V characteristics. This same device was stored in a nitrogen flow for about seven months. Then the device was mounted in an oil-free high vacuum ion system at 10^{-8} torr and baked at 100°C for approximately 120 hours. After this treatment, the measured C-V data was as shown in Figure 5. By comparing this data with that of Figure 4, one can see that the device characteristics are improved; the flatband voltage is reduced, the transition (from the accumulation region to the strong inversion region) is more abrupt, and the capacitance "knee" is sharper. The device was then exposed to air and annealed again in the same vacuum system (low 10^{-8} torrs) at about 100°C for 70 hours. Figure 6 shows the C-V data after this rebaking; note that the C-V data of the second annealing is practically identical to that of the first bakeout. The same device was kept in the high-vacuum without exposure to air for about three months and remeasured; the data, shown in Figure 7, shows that the device characteristics were not changed at all. These results indicate that annealing InSb MIS structures in high-vacuum improves device characteristics significantly.

We performed a high-vacuum annealing experiment on a line array of InSb MIS devices. The results are shown in Figure 8; the C-V curves for the eight units of the array were measured after the vacuum annealing.

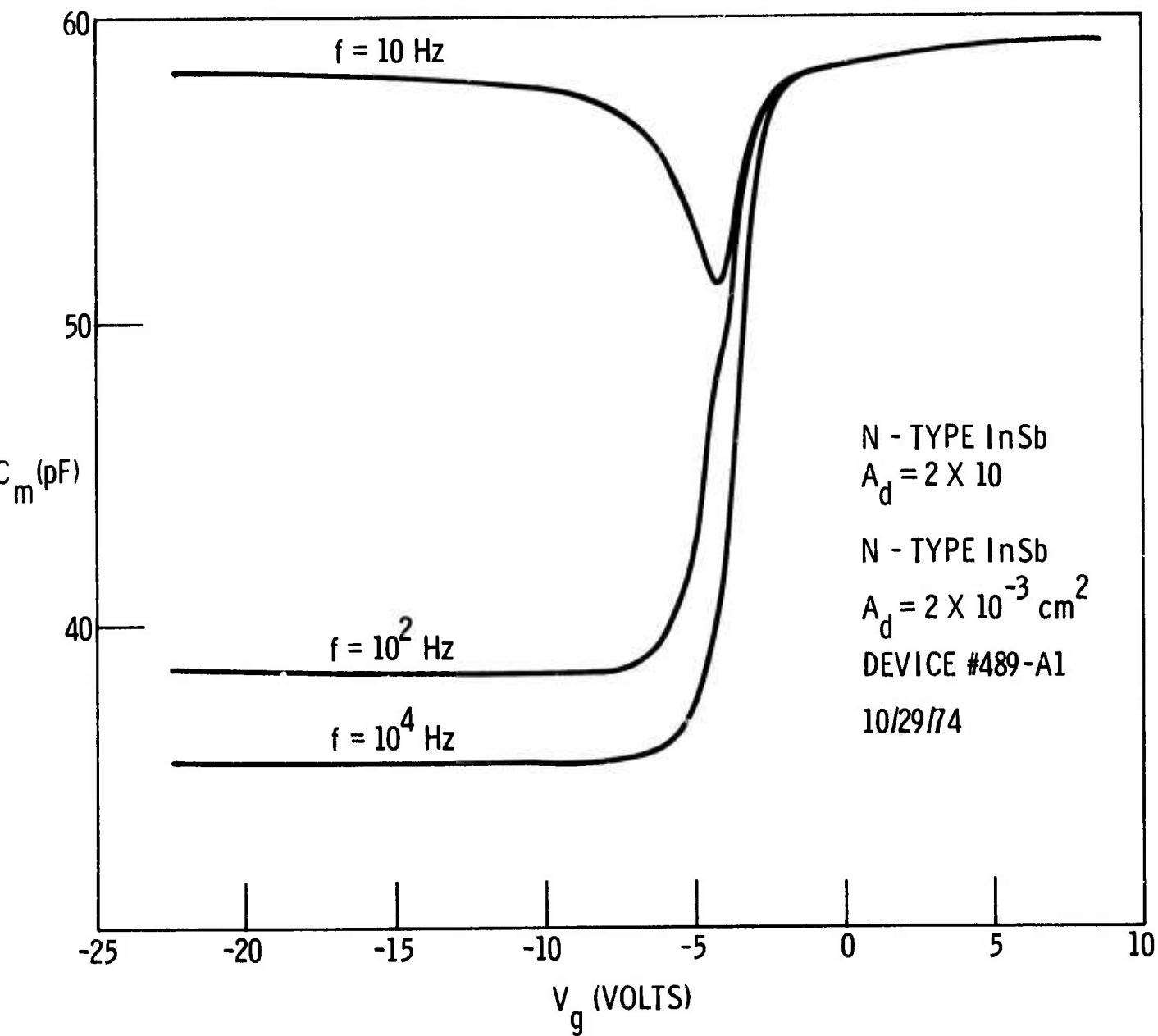


Figure 4. C-V Data Measured in Poor Vacuum
Right After Device Fabrication

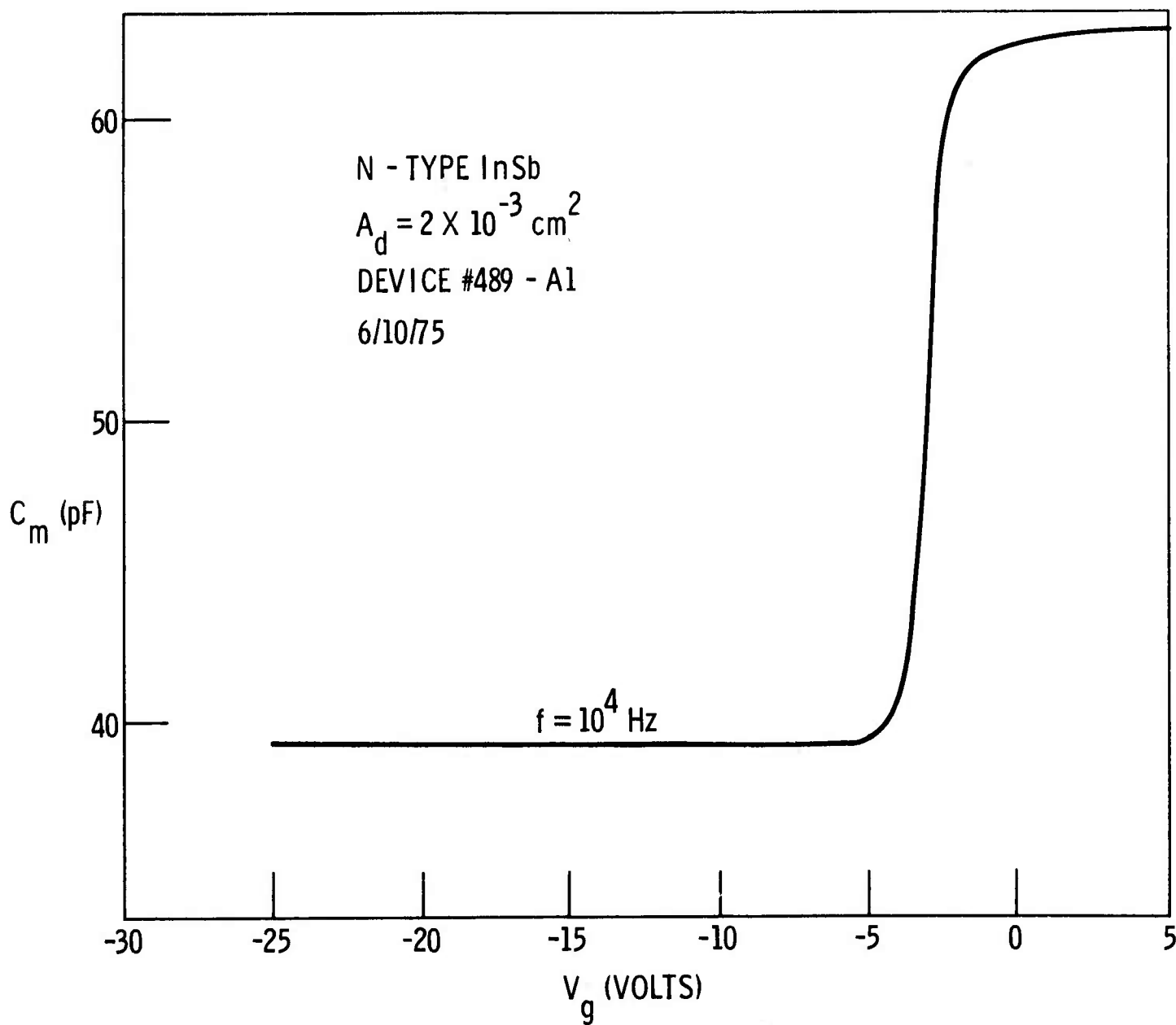


Figure 5. C-V Data After Baking at 100°C
for About 120 Hours in High Vacuum.

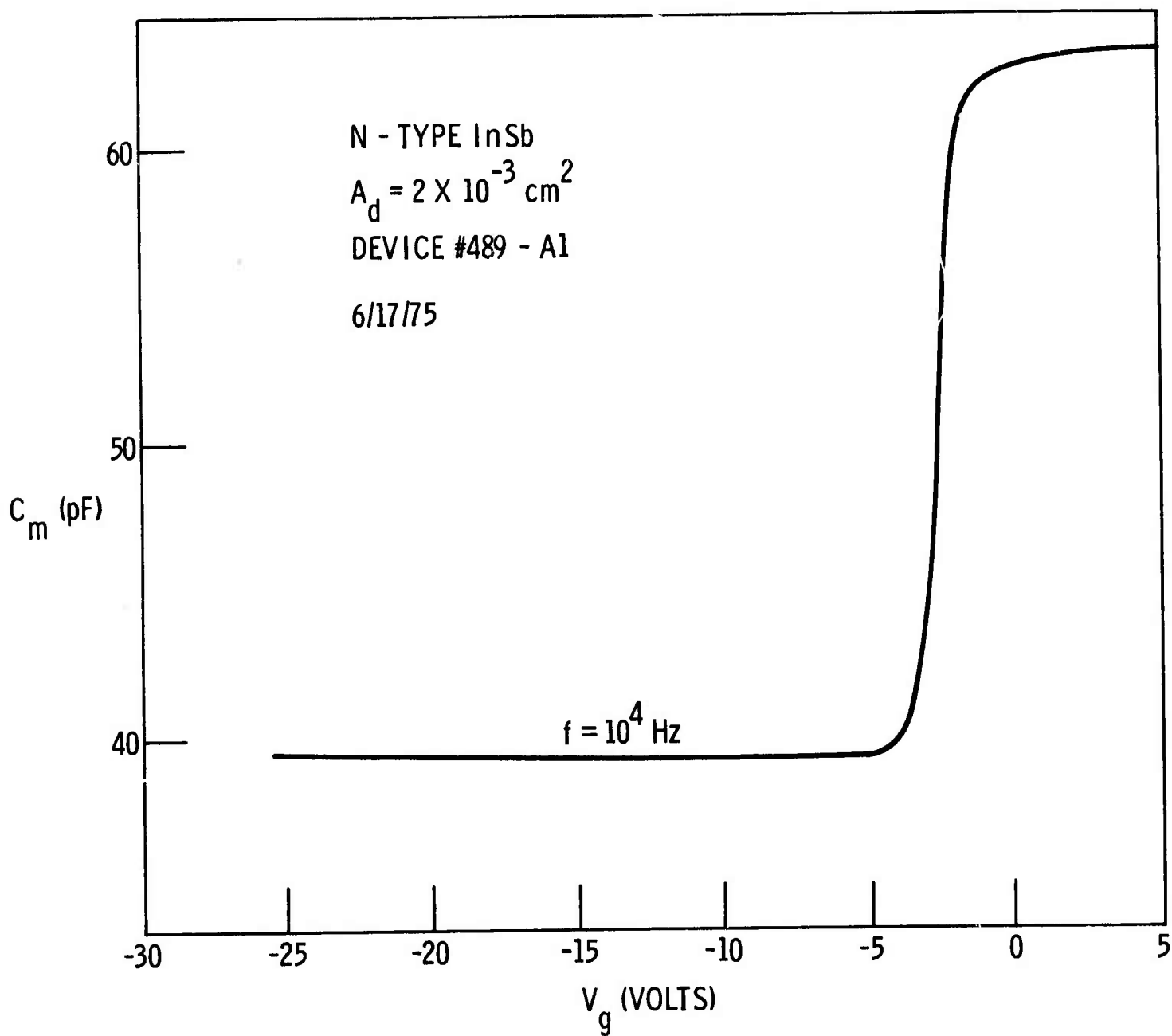


Figure 6. C-V Data After Exposure to Air and Re-Baking at 100°C for About 70 Hours in High Vacuum.

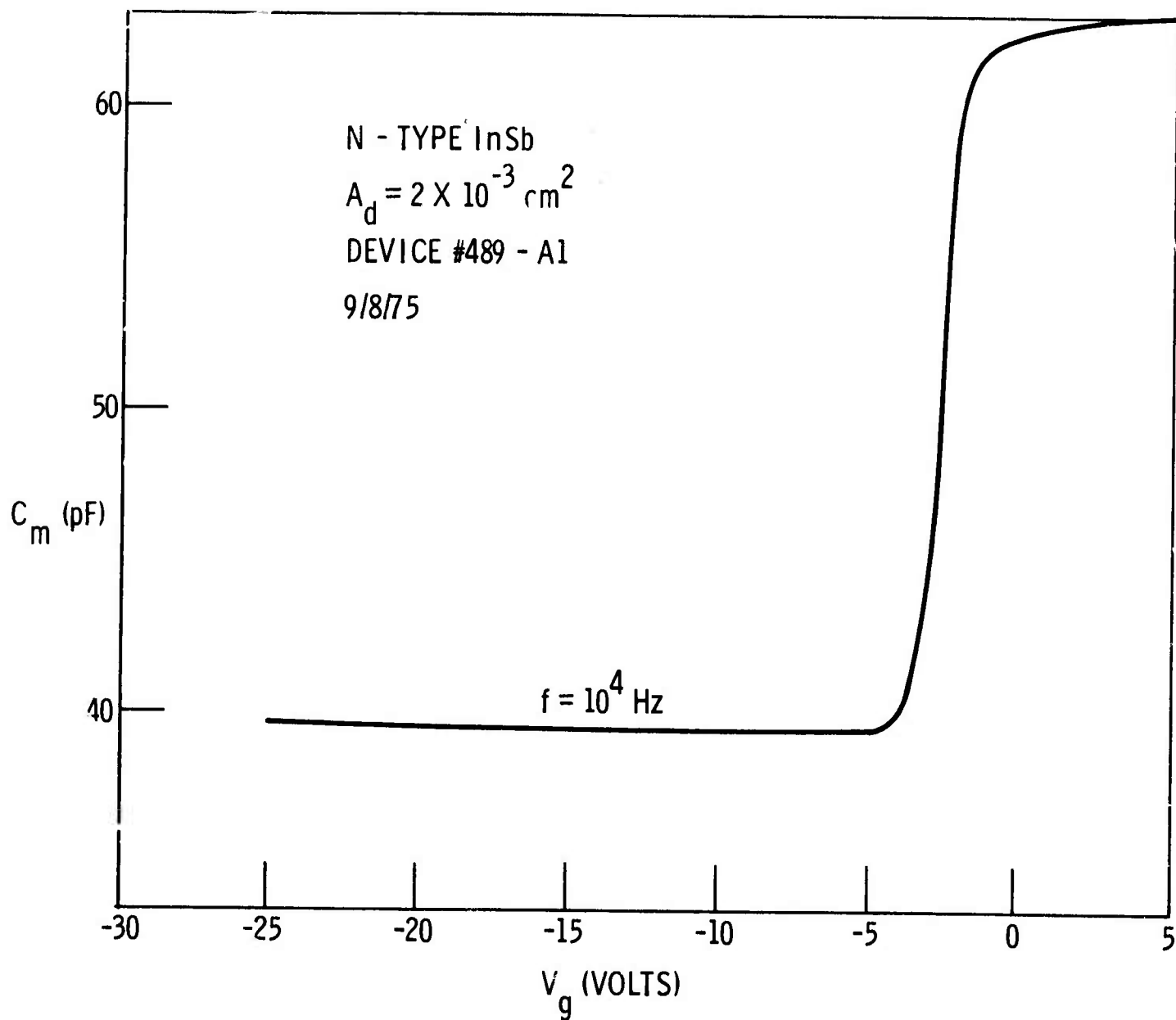


Figure 7. C-V Data Re-measured After Storing
in the Same Vacuum for Three Months.

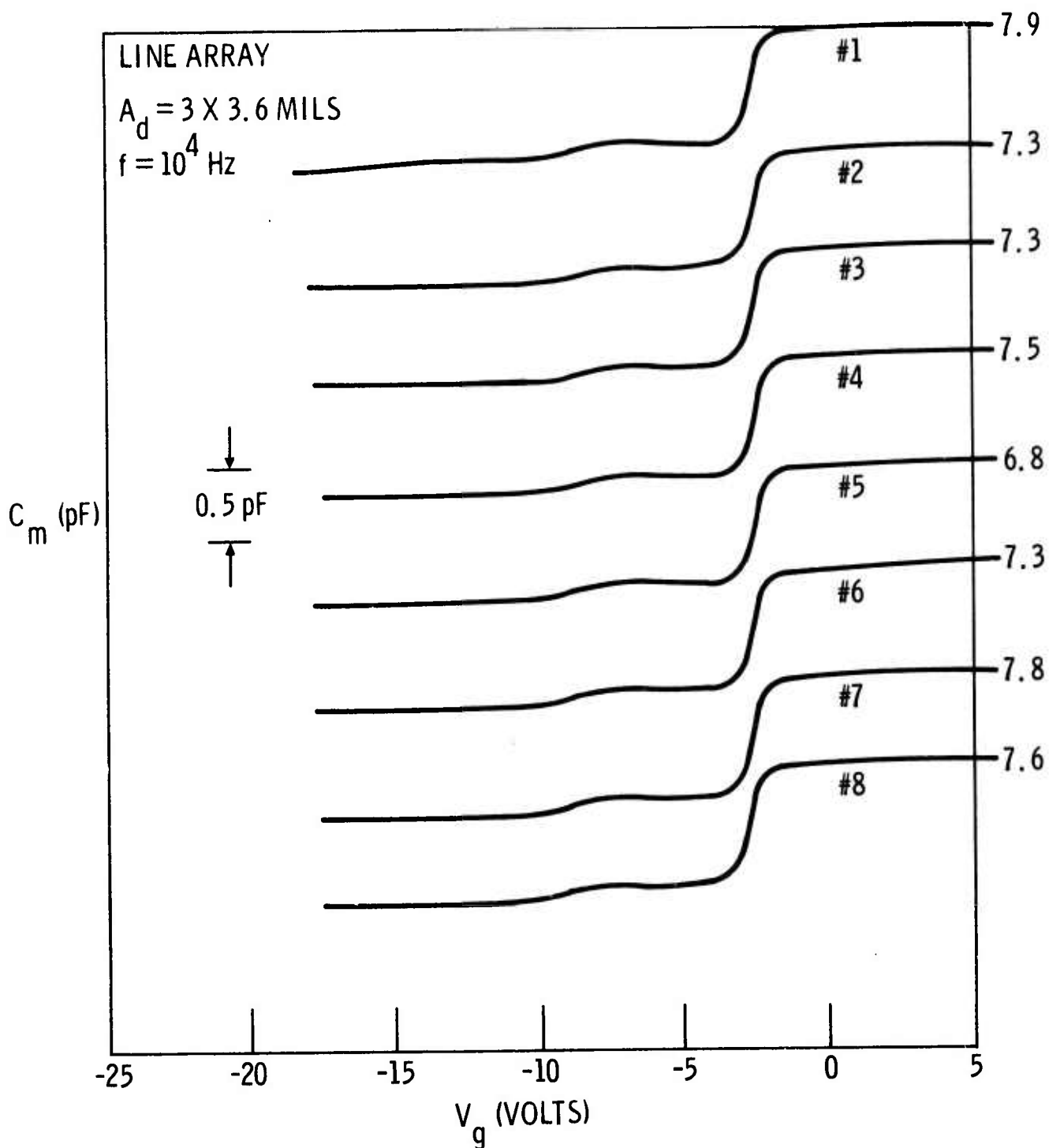


Figure 8. C-V Data of a Line Array After Baking at 105°C for Six Days in High Vacuum.

Note that the flatband voltage of all 8 devices is the same, thus resulting in uniform device characteristics. This array was fabricated using a photoresist and wet chemistry technique, and the lead contact to the active gate areas was made on a thick field oxide. The slight bump patterns in the strong inversion region may be due to a slight depletion under the field oxide. This will be reported on later.

The interface state properties of the high vacuum annealed InSb MIS structures were investigated quantitatively. The C-V data are shown in Figure 9. The dotted line represents the C-V curve derived from theory and calculated by a computer⁽⁷⁾. As shown, the flatband voltage is about 2.5V and the high-frequency experimental C-V curve closely follows the theoretical curve, especially near the flatband voltage region where all of the curves measured at different frequencies coincide. This indicates a low surface state density.

In order to determine the interface state densities of these devices more accurately, we used a conductance technique⁽⁸⁾. Typical conductance voltage characteristics for the high-vacuum annealed InSb MIS structures are shown in Figure 10. The rise in conductance in certain bias regions is due to the carrier flow by the interface states. Thus the conductance values in the peak region can be related to the interface state density. Note that the conductance values shown in Figure 10 are an order of magnitude lower than those presented earlier⁽⁹⁾.

In the surface state activated bias region (the peak conductance region), a simplified equivalent circuit^(8,10) can be derived, as shown in Figure 11; here C_o is the oxide capacitance, C_D is the depletion capacitance, and the capacitance, C_s , and resistance, R_s , are associated with the surface states and can be derived from the Shockley-Read-Hall statistics for majority carriers⁽¹⁰⁾. The C_s and R_s in the surface state branch of the equivalent circuit of Figure 11 can be further modified as a parallel combination, as illustrated in Figure 12, where C_{ss} and G_{ss} are now both frequency dependent, as follows,

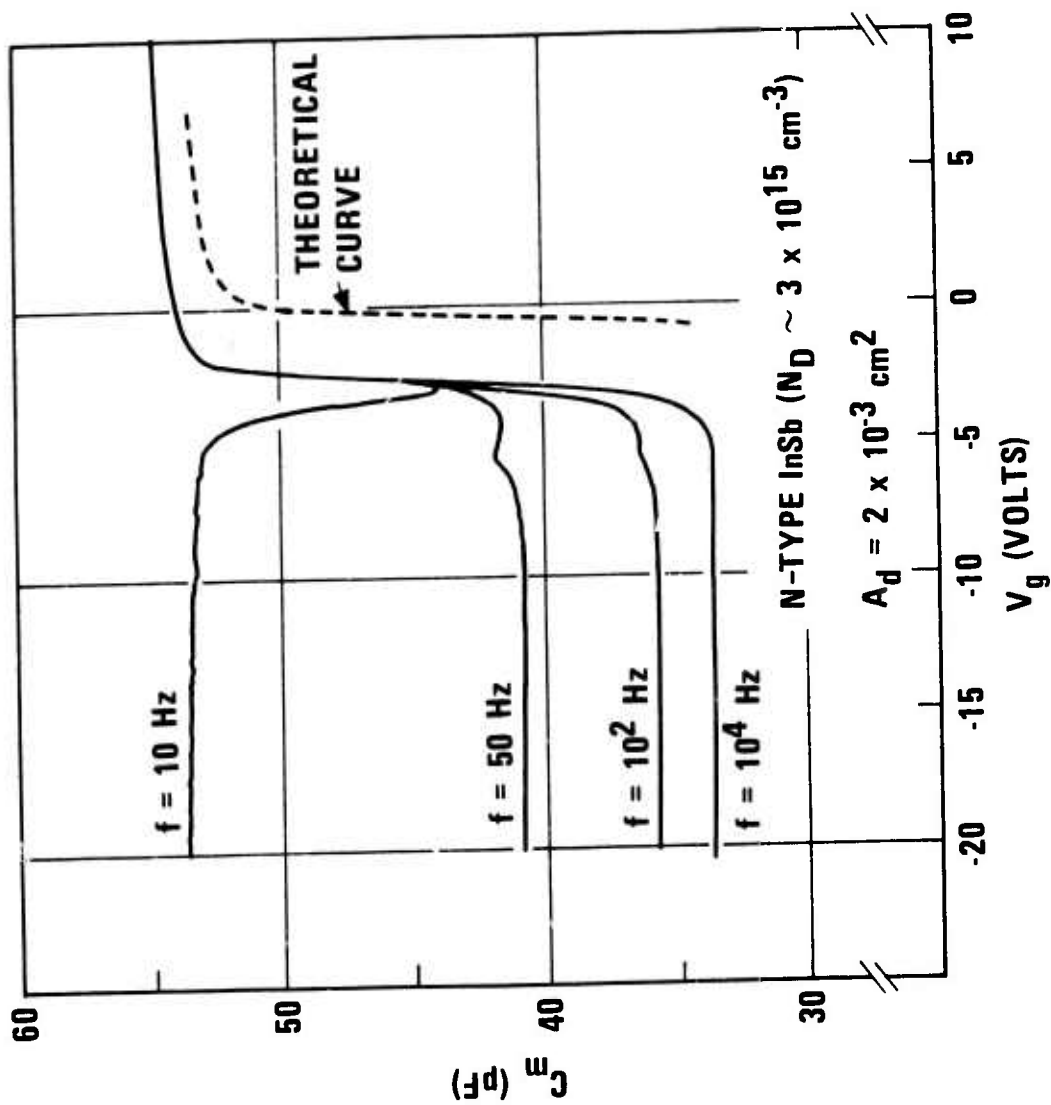


Figure 9. C-V Characteristics of InSb MIS Structure
 After High Vacuum Bake-Out.

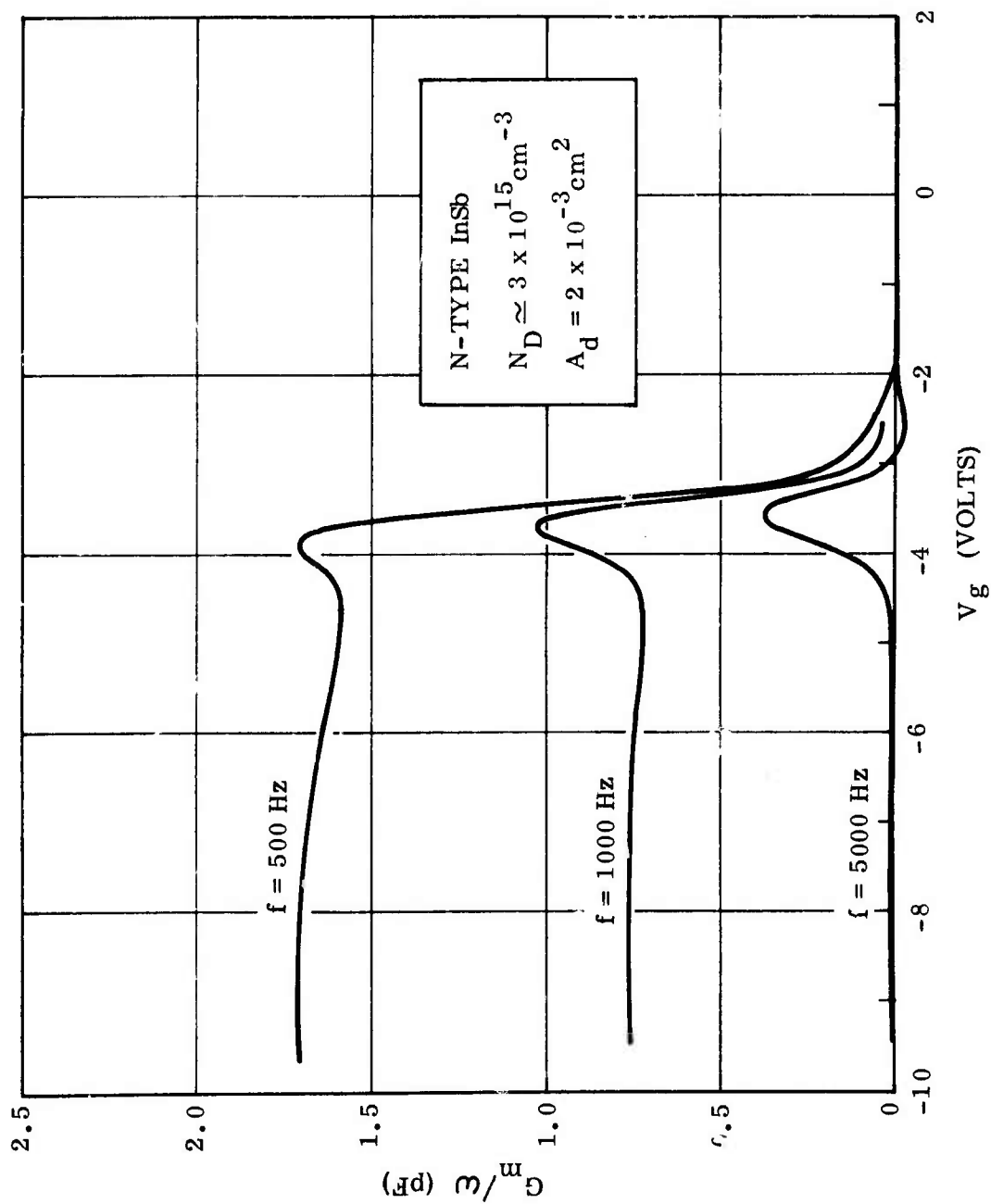


Figure 10. G_m/ω - Voltage Characteristics of InSb MIS Structure.

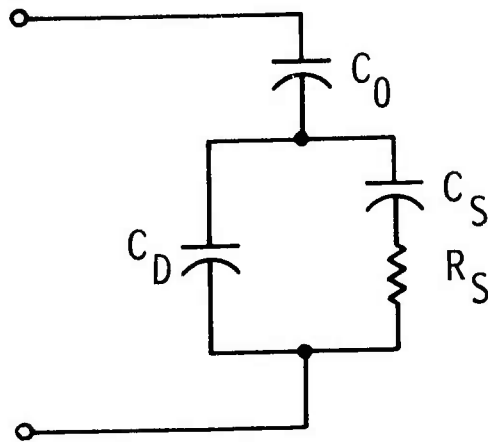


Figure 11. Simplified Equivalent Circuit for an MIS Structure Showing the Interface State Branch.

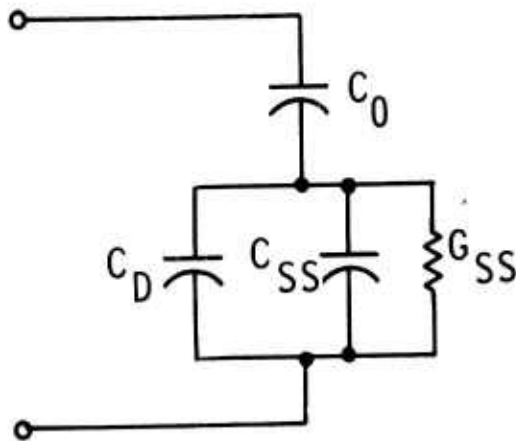


Figure 12. Parallel Representation of C_S and R_S of the Equivalent Circuit shown in Figure 11.

$$C_{ss} = \frac{C_s}{1 + (\omega\tau_s)^2} \quad (1)$$

$$\frac{G_{ss}}{\omega} = \frac{C_s \omega\tau_s}{1 + (\omega\tau_s)^2}, \quad (2)$$

where $\tau_s = R_s C_s$, the surface state time constant, and ω is the angular frequency for a small ac signal. The parallel branch of the equivalent circuit of Figure 12 can be simply represented by an equivalent parallel capacitance, C_p and an equivalent parallel conductance, G_p , where $C_p = C_D + C_{ss}$ and $G_p = G_{ss}$. Note that G_p depends only on the surface state branch, C_s and R_s , whereas C_p is a function of both C_D and the surface state branch. Therefore, the equivalent parallel conductance values should yield more reliable and accurate values of the interface state densities.

The values of C_p and G_p can now be easily determined as a function of the measured terminal capacitance, C_m and conductance, G_m (we actually measure G_m/ω directly at given frequencies). Thus, via the equivalent circuits of Figures 11 and 12 one can obtain C_p and G_p/ω as a function of C_m and G_m/ω , respectively,

$$C_p = \frac{C_o \left\{ C_m^2 + \left(\frac{G_m}{\omega} \right)^2 \right\} \left\{ C_m (C_o - C_m) - \left(\frac{G_m}{\omega} \right)^2 \right\}}{\left(\frac{C_o G_m}{\omega} \right)^2 + \left\{ C_m (C_o - C_m) - \left(\frac{G_m}{\omega} \right)^2 \right\}^2} \quad (3)$$

$$\frac{G_p}{\omega} = \frac{\frac{C_o^2 G_m}{\omega} \left\{ C_m^2 + \left(\frac{G_m}{\omega} \right)^2 \right\}}{\left(\frac{C_o G_m}{\omega} \right)^2 + \left\{ C_m (C_o - C_m) - \left(\frac{G_m}{\omega} \right)^2 \right\}^2} \quad (4)$$

A simple computer program of the above equations was written and the values of C_p and G_p/ω were calculated using the measured values of C_o , C_p , and G_m/ω , as obtained from the C-V and G-V data (Figures 9 and 10, respectively). That is, at given bias points in the peak conductance region, the values

of C_m and G_p/ω were measured as a function of frequency from the admittance measurements and, thus, the equivalent parallel conductance values, G_p/ω , versus frequency were determined.

If the G_p/ω versus frequency follows Equation (2), the surface state density can be determined by the single-time constant model, in which case the peak value of G_p/ω is simply equal to $C_s/2$ at $\omega\tau_s = 1$. Then the interface state density N_{ss} is given by,

$$N_{ss} = \frac{C_s}{q A_d}, \quad (5)$$

where q is the electronic charge and A_d is the gate plate area of the MIS structure. Therefore, the G_p/ω versus frequency data yield the surface state density, N_{ss} , and its time constant, τ_s . At certain bias points, however, the G_p/ω frequency curve does not always follow Equation (2) but, rather, fits the following equation⁽⁹⁾,

$$\frac{G_p}{\omega} = \frac{qN_{ss}A_d}{2\omega\tau_m} \ln(1 + \omega^2\tau_m^2), \quad (6)$$

which was derived from a continuum model⁽¹¹⁾, in which τ_m is the time constant for a continuum of states. It was assumed that since many single-level states were very closely spaced in energy across the bandgap at the surface, the surface states appeared as a continuum over the bandgap. Thus, the total admittance can be obtained by summing up the admittance of all the states. Equation (6) was obtained by integrating the conductance, (Equation (2)) for a single-level state with respect to bandgap⁽¹¹⁾.

For our InSb MIS structures, the measured G_p/ω - frequency curves follow only the two models discussed above, either the single time constant or continuum model, depending on the bias region. These experimental curves have been previously reported⁽²⁾, for example at different bias points in the peak conductance region, we have extracted the G_p/ω - frequency data from the admittance measurements. From these data, then, we can obtain a relationship for the surface state density versus bias and,

then, plot the surface state density as a function of surface potential. The values of surface potential at each bias point were obtained by comparing the theoretical C-V curve with the high-frequency experimental C-V data, as shown in Figure 9.

Figure 13 shows the experimentally determined surface state density (N_{ss}) versus surface potential (Φ_s). The circle-dot points represent the values determined by the continuum model, whereas the triangle points were obtained from the single time constant model. The intrinsic level (E_i) is also indicated in the figure. As one can see, in the depletion region the experimental results follow the continuum model, but in the weak inversion region the measured data fit the single time constant model. The surface state density varies from mid- $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ to about mid- 10^{11} in the range measured. Note that the surface state density tends toward a minimum value near the flatband ($\Phi_s = 0$); this result is also shown in the C-V data of Figure 9, where, near the flatband voltage region, the C-V curves measured at different frequencies coincide and more closely follow the theoretical curve, an indication of a lower surface state density.

The result of a minimum surface state density near the flatband region for InSb MIS structures is different from that observed in the Si-SiO₂ MOS system, where the minimum surface state density is near the intrinsic level (mid-band)⁽¹⁰⁾. It is also interesting that, for the Si-SiO₂ MOS system, the measured equivalent parallel conductance values cannot be described by Equation (6) at any bias points. In the depletion bias region, the G_p/ω data had a much broader dispersion in frequency than that of Equation (6) and, in order to fit the experimental values of G_p/ω , the continuum model, Equation (6) was further modified on the basis of a statistical model⁽¹⁰⁾. As shown in Figure 13, for the InSb MIS system, the continuum model alone was capable of characterizing the G_p/ω -frequency data in the depletion region. In our earlier report⁽²⁾, however, G_p/ω -frequency data did not fit any model in the depletion region. These InSb MIS structures had not been annealed in high-vacuum, and the present high-vacuum annealed structures are, thus, definitely improved and yield a more complete picture of the interface state properties.

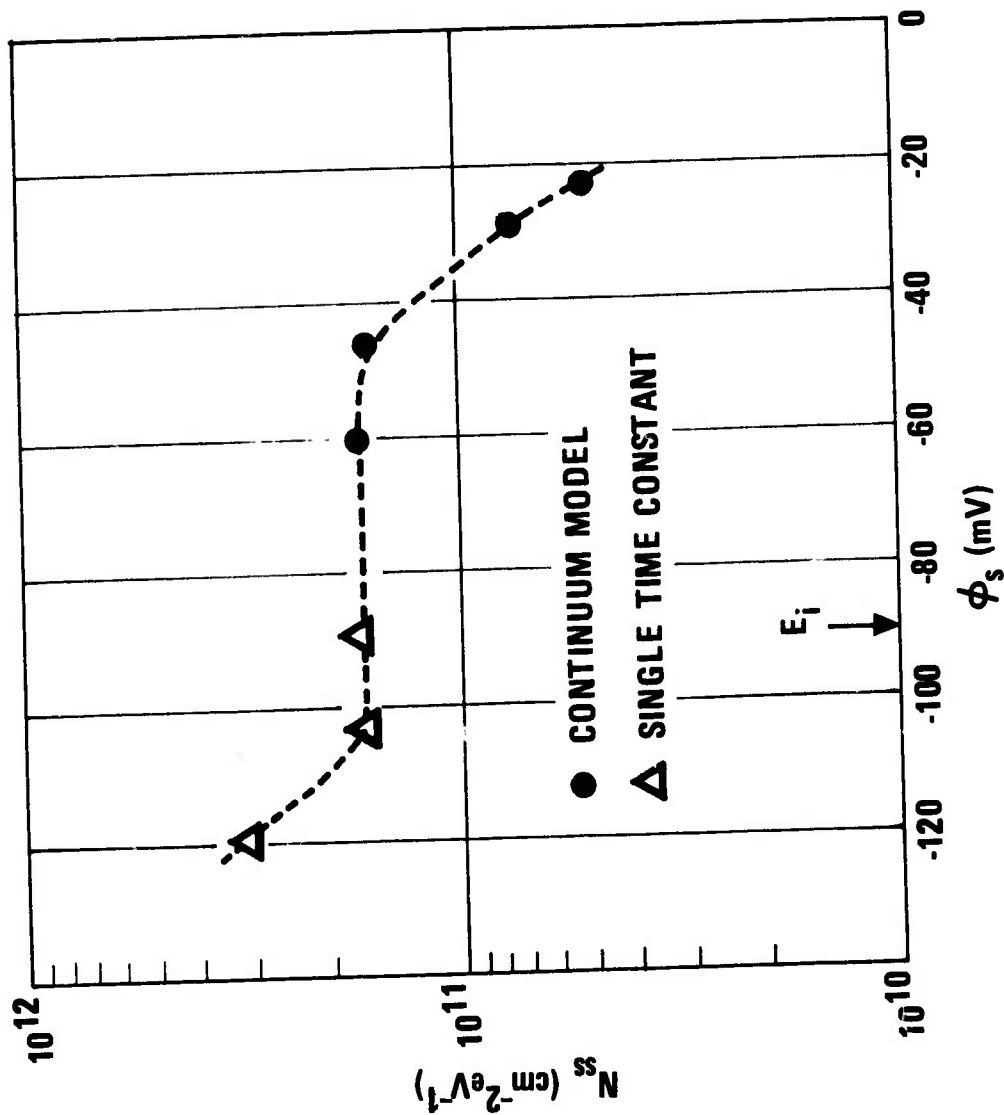


Figure 13. Surface State Density (N_{ss})
VS Surface Potential (ϕ_s)

The surface state time constant values can be determined from the G_p/ω - frequency data since, for the single time constant model, it has a peak at $\omega\tau_s = 1$, and for the continuum model, the peak occurs at $\omega\tau_m = 1.98$. Thus τ can easily be found. The surface state time constant values corresponding to the surface states shown in Figure 13 are shown in Figure 14. The separate data points represent the two models, respectively. In both cases the time constant varies exponentially with the surface potential, but with different slopes. For the continuum model the slope is $\beta/2$, whereas for the single time constant case, it is $\beta/4$, where $\beta = q/kT$. An extrapolation of the two lines, however, meets at about the same points in the flatband voltage.

If the capture cross-section is independent of energy then the slope should be equal to β . A slope smaller than β may be due to the fact that the capture cross-section is energy dependent. For the single time constant data, an even slower increase in the time constant may be due to an additional contribution of minority carrier generation.

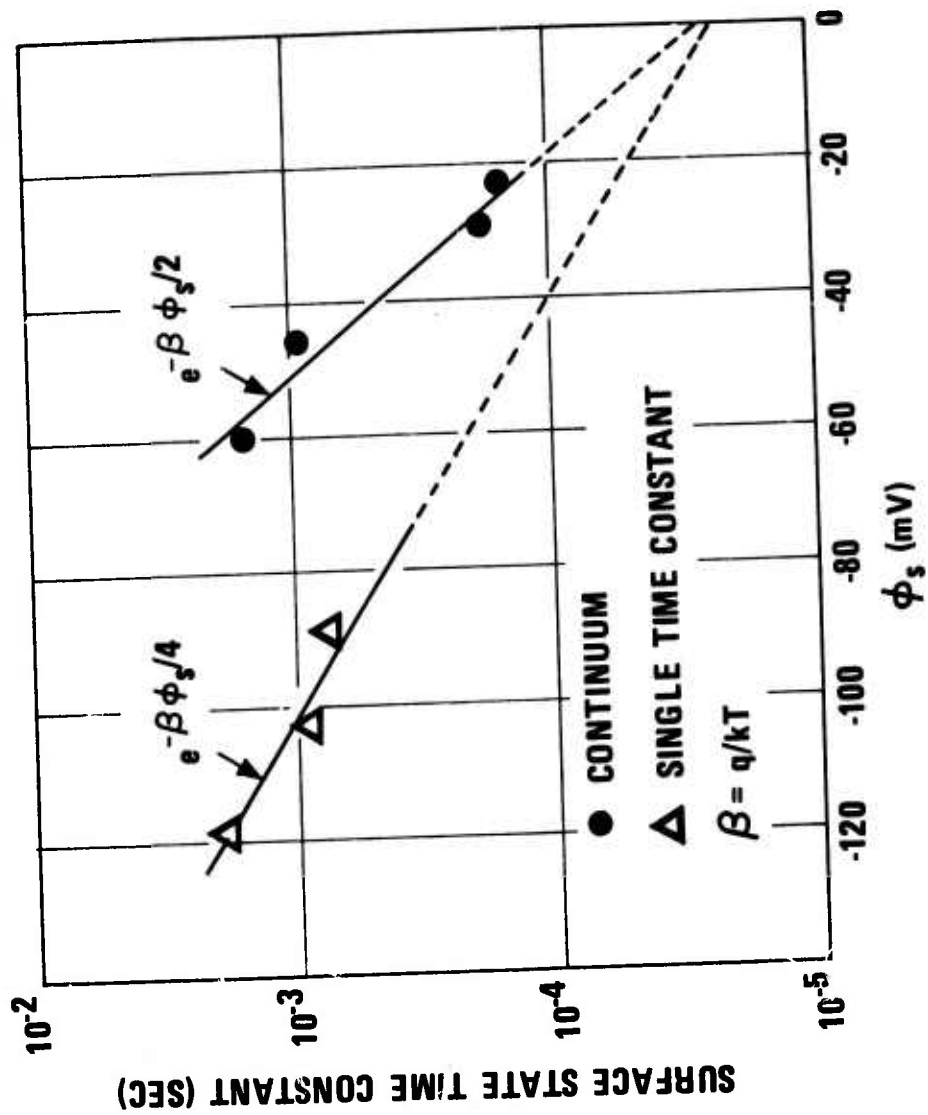


Figure 14. Surface State Time Constant vs Surface Potential.

IV. MEASUREMENTS OF HIGH SENSITIVITY InSb CID LINEAR ARRAY

1. Measurement Setup

The InSb MIS/CID imaging device technology has progressed rapidly to the point where high-sensitivity InSb CID devices have been realized. We present here sensitivity measurements and experimental results for an InSb CID line array and then compare these results with the theoretical values. The noise sources of the device are also discussed.

Figure 15 shows the detailed setup used for the sensitivity measurements. A line array of InSb CID was used together with a 32-stage silicon shift register scanner. Only three elements of the array were connected to the silicon scanner stages (Nos. 13, 15 and 17, respectively), as shown on the left-hand side of Figure 15. The last stage of the scanner, No. 32, was used but it was connected to a 2 pF capacitor to measure other noise components of the system.

All of the unused scanner stages were left open. The silicon scanner and InSb CID devices were mounted on a common substrate and operated at the same temperature, near 77°K. The reset switch and preamplifier in the dewar were also operated at the same temperature but the injection coupling capacitor (5 pF), located inside the dewar, was not.

Ten wire leads interconnected the devices through the dewar (one of these was a ground lead). Thus the measurement setup, essentially, operates as a focal-plane line array.

To clock the scanner, the input, Φ_1 and Φ_2 , pulses of the silicon shift register were adjusted to scan all of the 32 stages for one ms; thus, the integration time for the InSb devices is one ms, which requires a sampling rate of 32 kHz in the first sample-and-hold circuit. The preamplifier voltage gain was set at about 25, and the sampled signal was further amplified at a gain of 10. In order to select one element at a time, a second sample-hold circuit with a sampling rate of one kHz was used.

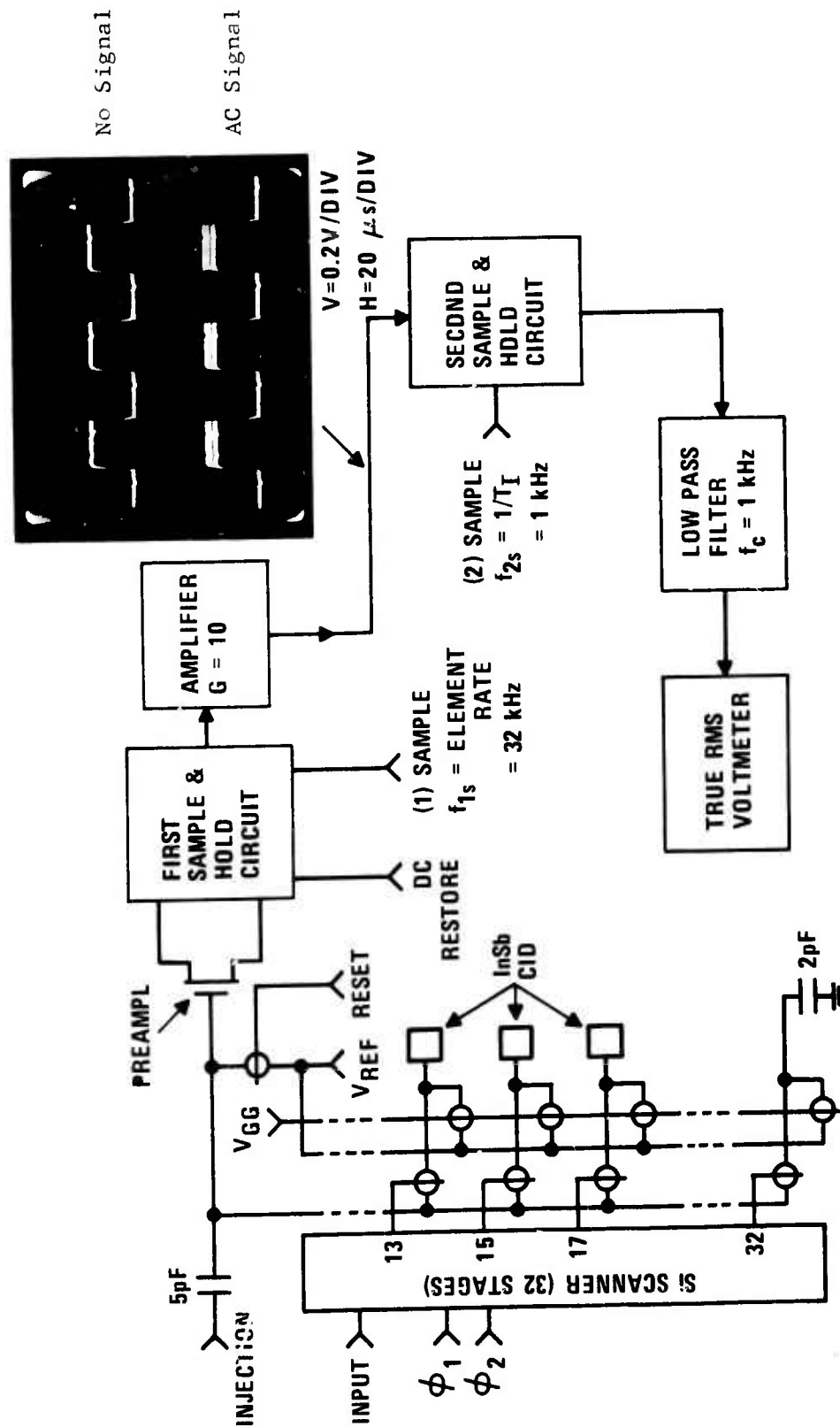


Figure 15. Experimental Setup Used in the Sensitivity Measurements of InSb CID Line Array.

The output signal of the second amplifier is displayed in the photograph of Figure 15. The three positive pulses are due to the three InSb CID devices, that is, the response of the Nos. 13, 15 and 17 output stages of the silicon scanner. They move in a positive direction because of the CID capacitance. The output signals also move in a positive direction because the device capacitance increases with increasing signal. The upper trace represents the no-signal case; in the bottom trace the multi-lines represent the signal generated from a blackbody source using a chopper*. The ac signal displayed above the three pulses, in the bottom trace, demonstrates the uniformity of the three InSb CID devices. If we connect more InSb devices to the stages of Nos. 14, 16, etc., we will obtain a continuous signal.

In order to measure the signal and noise voltages of a particular element in the array more quantitatively, a second sample-and-hold circuit with a sampling rate of 1 kHz was introduced. For the InSb CID, we selected the No. 13 stage of the silicon scanner. The peak-to-peak signal values were then displayed and measured, using a chopper as described above. The rms noise was measured with a true rms voltmeter followed by a low-pass filter, as illustrated in Figure 15. The cutoff frequency of the low-pass filter was set at 1 kHz, twice the Nyquist limit, to assure that all of the noise passed through.

It should be pointed out that the effective noise bandwidth is not the cutoff frequency of the filter, 1000 Hz, but 500 Hz, the Nyquist limit. We will show later that, for the D^* calculation, the noise bandwidth is equal to 500 Hz, though the filter bandwidth is 1000 Hz.

The first stage preamplifier has a large bandwidth (1 - 2 MHz) so that the injection pulse can be recovered for signal sampling. The injection pulse width was about 3 μ s. The 3 db cutoff frequencies of the two sample-and-hold circuits were made much higher than the respective Nyquist frequencies.

* While the chopper was not absolutely necessary, it does facilitate the measurements. If the chopper is not used, the signal is the difference between the two traces shown in Figure 15.

2. Noise Sources of the System

A major source of noise in the system is the kTC noise, caused by the reset switch. However, this noise component can be removed completely using the double-correlated sampling technique shown in Figure 16, which is the equivalent circuit for the enable-line readout used in the measurement setup of Figure 15. During each element time, the amplifier sensing line is reset to the reference voltage, V_{REF} , and allowed to float. This operation causes a kTC noise, a voltage uncertainty on the sensing line, which, however, can be removed via a restore switch after the signal amplification, as illustrated in Figure 16. The operation is as follows: immediately after the reset switch has been opened, the dc restore switch is closed to absorb the kTC offset voltage across the restore capacitor, thus eliminating this noise component. All of the appropriate waveforms used for the measurements are shown in Figure 17. (The sampling pulses for the second sample-and-hold circuit are not shown).

After removing the kTC noise, we can measure the other noise components, 1) amplifier noise, 2) select switch thermal noise, 3) dark current shot noise, and 4) shot noise due to the background photon flux incident on the InSb devices. The amplifier and select switch thermal noises are combined as an amplifier noise and measured together. All other noise sources are measured separately. The total number N_{TN} of rms noise carriers is given by

$$N_{TN}^2 = N_{amp}^2 + N_{DN}^2 + N_{BN}^2, \quad (7)$$

where N_{amp} is the combined select switch and the amplifier noise, N_{DN} is the dark current shot noise, and N_{BN} is the shot noise of the background photon flux.

The amplifier noise, N_{amp} , can be measured simply by selecting the scanner stage No. 32, which was connected to a 2 pF capacitor. Thus, the shot noise of the dark current and background, N_{DN} and N_{BN} , are equal to zero. The total number of rms noise carriers in this case is equal to N_{amp} ,

$$N_{TN} = N_{amp}. \quad (8)$$

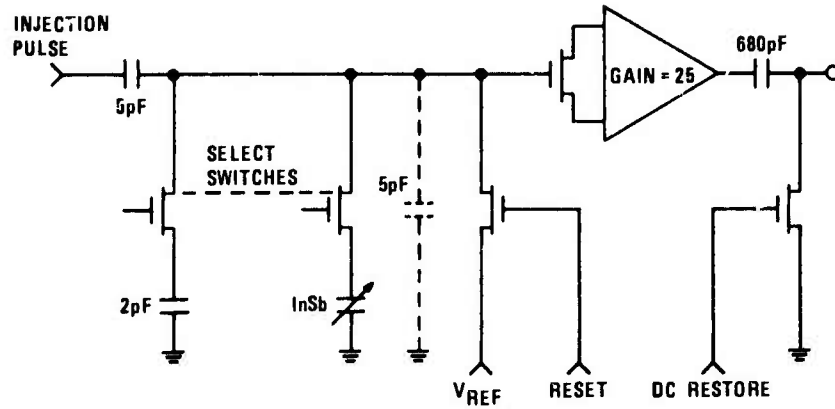


Figure 16. Equivalent Circuit for the Enable-Line Readout Used in the Measurement Setup Shown in Figure 15.

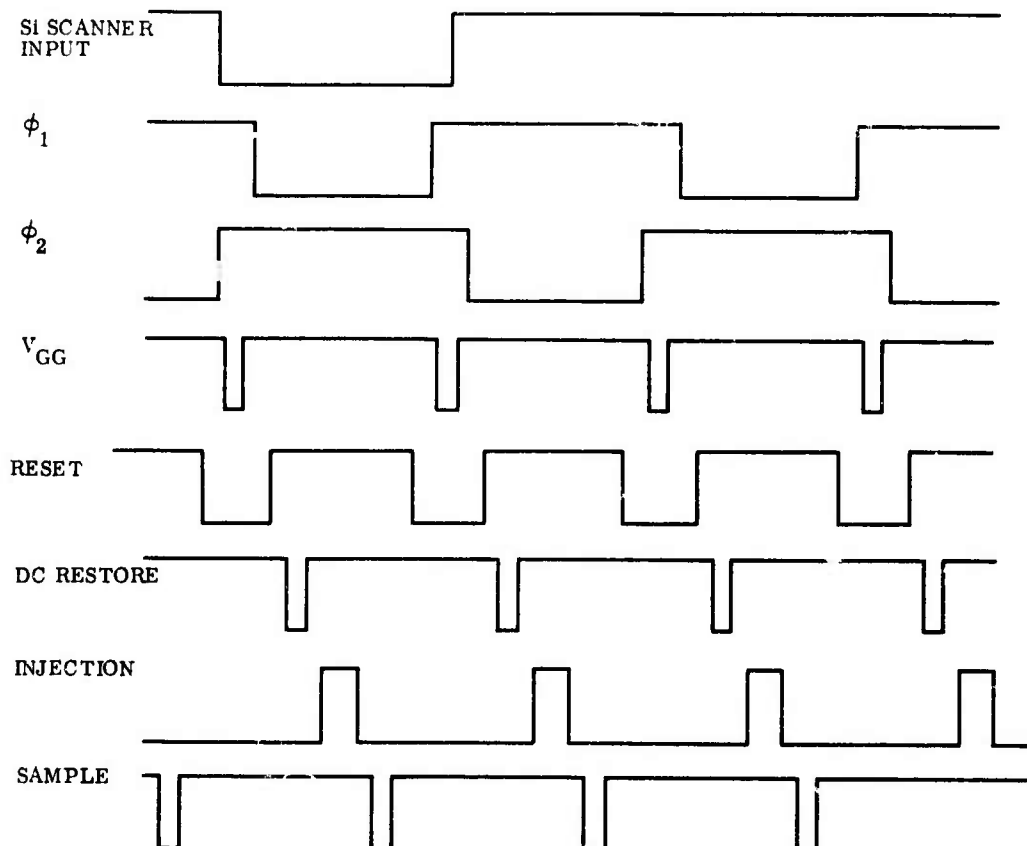


Figure 17. Operating Pulse Waveforms Used in the Measurement Setup Shown in Figure 15.

The dark current shot noise, N_{DN} , is determined by measuring the total noise while shielding the InSb devices from the background photon flux ($N_B = 0$) when selecting a stage connected to the device (for example, stage No. 13, 15 or 17). The total number of rms noise carriers is, then,

$$N_{TN}^2 = N_{amp}^2 + N_{DN}^2. \quad (9)$$

Since N_{amp} is known from Eq. (8), we can determine the rms noise carriers of the dark current shot noise and, then, measure the rms noise carriers (N_{BN}) due to the background photon flux from Equation (7).

3. Transfer Characteristic

For the system transfer function measurements, we used a 500°K blackbody source and a cooled narrow spike filter with known transmission data (see Figure 18). The peak transmission is about 80% at 4.18 μ m with a half-width of approximately 0.1 μ m. These data were supplied by the vendor and measured at room temperature. However, our previous measurements of the transmission curve for this type of filter showed, essentially, the same transmission values at 77°K. The filter and the device were both attached to the same cold finger inside the dewar and, so, on cooling both should be at the same temperature, i.e. $\sim 77^\circ\text{K}$. In addition, a cold aperture with different field-of-view angles was used to control the background photon flux.

The input signal photons were computed on the basis of the blackbody source temperature (500°K), the distance from the source to the device, and the transmission data. The input signal intensity was varied by changing the distance. Figure 19 shows a typical transfer characteristic, the output signal voltage as a function of the number of input signal carriers (the measurement conditions are given in the upper left-hand side of the figure). The circled points are the experimental results and, as expected, are quite linear. The rms noise voltage of the system was also measured by blocking the blackbody source from the device; the result is shown on the extrapolated straight line in Figure 19. These results, then, directly yield the number of rms noise-equivalent carriers (NEC), which is, from

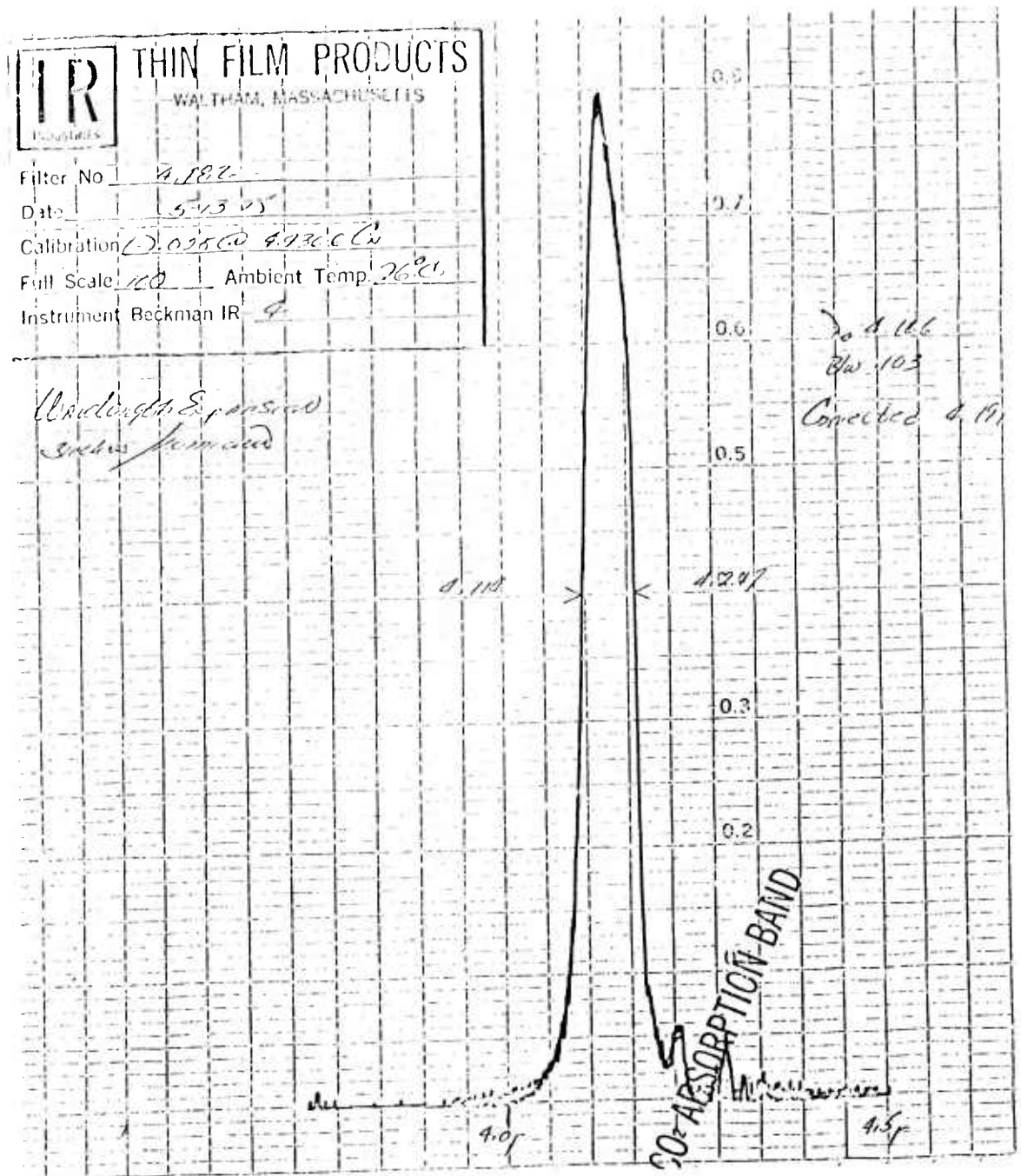


Figure 18. Transmission Curve of a 4.18 μm Spectral Filter Used in the Sensitivity Measurements.

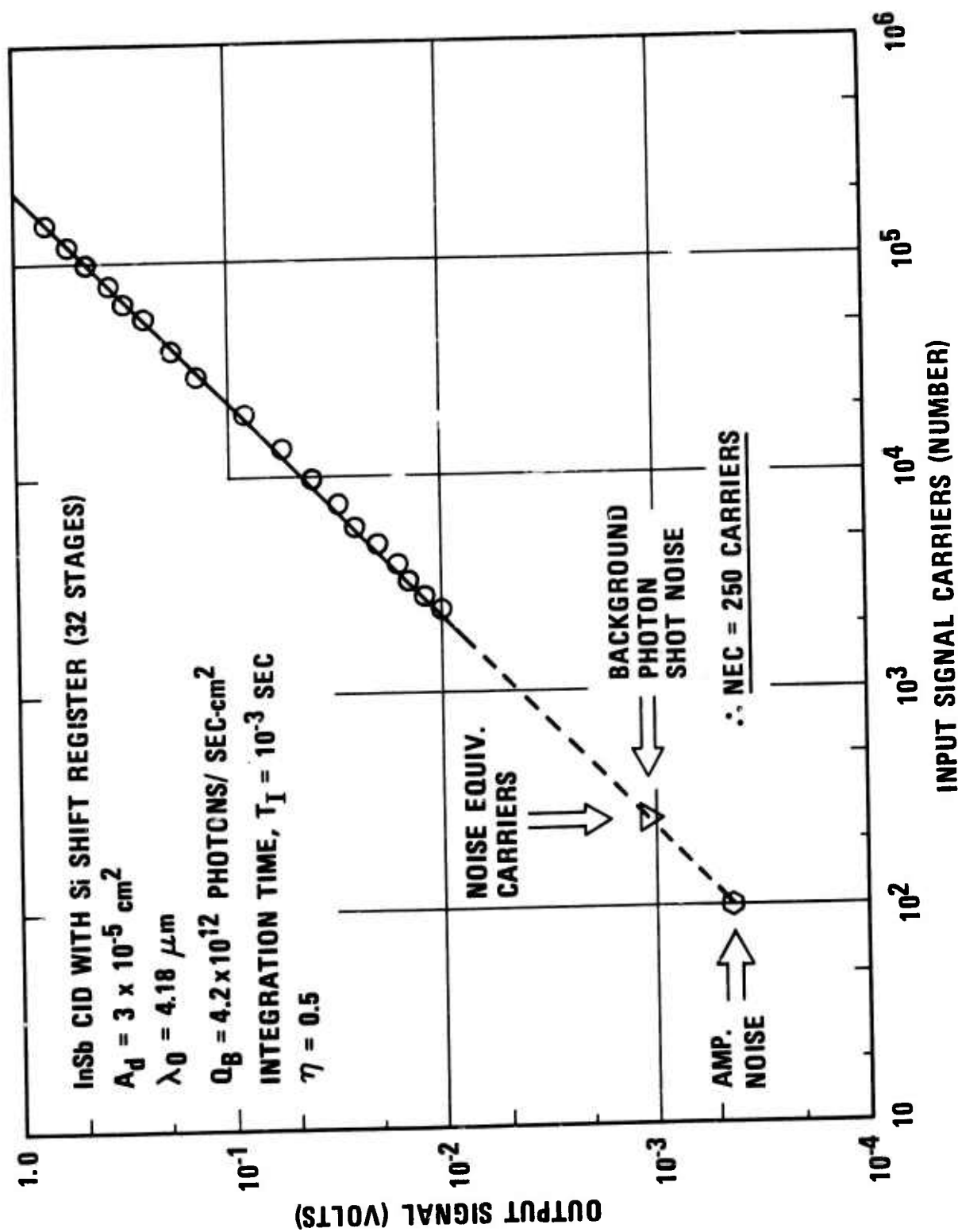


Figure 19. Transfer Characteristic of InSb CID Line Array.

Figure 19, 250. The amplifier noise voltage, measured using the No. 32 stage of the silicon scanner, yielded a value of 100 for rms amplifier noise carriers. For any measured rms noise voltage, therefore, one can simply determine the number of rms noise-equivalent carriers from the transfer curve of Figure 19. We have measured the same transfer characteristic at different background levels.

The approximate transconductance, g_m , of the preamplifier MOSFET device was calculated, based on the device dimensions and the mobility value at 77°K, as 5000 μ mhos. With a cascoded preamplifier circuit and $R_L = 5$ kohms, the preamplifier voltage gain was about 25. Since the gain of the second amplifier is 10, the overall voltage gain is 250. (These values correspond to the experimental results shown in Figure 19.) The measured responsivity is 4×10^{-6} volts/carrier and, thus, at the input (sensing line) it is 1.6×10^{-8} volts/carrier. The signal voltage, V_s , is approximately,

$$V_s \approx qN/C_{in}, \quad (10)$$

where q is the electronic charge, N is the number of signal carriers, and C_{in} is the total input capacitance (the injection pulse coupling capacitance plus the sensing line and the preamplifier input capacitance, 10 pF). Therefore, the responsivity, q/C_{in} , is 1.6×10^{-8} volts/carrier, which is, indeed, the same as the measured value.

The capacitance on the sensing line was measured as follows. The preamplifier transistor was used as a source-follower configuration (R_L was outside the dewar) to measure the injection pulse voltage on the sensing line; then it was compared to the input injection pulse voltage. The sensing line capacitance was thus determined to be about 5pF, as indicated in Figure 16.

4. Background Limited Performance

The number (N_B) of carriers generated by the background photon flux is

$$N_B = \eta Q_B A_d T_1, \quad (11)$$

where η is the quantum efficiency, Q_B the background photon flux density incident on the device, A_d is the active device area and T_I is the integration time. Thus, for the data of Figure 19, N_B is equal to 6.3×10^4 carriers.

The background shot noise, N_{BN} , is simply the square root of the background generated carriers,

$$N_{BN} = (N_B)^{1/2} \quad (12)$$

thus, the number of rms noise carriers due to the background photon flux is 250. The number of noise equivalent carriers (NEC) is, therefore, equal to the shot noise of the background carriers, indicating that the performance is background limited.

Using the conventional D^* notation for IR detectors,

$$D_{\lambda_0}^* \text{ (measurement)} = \frac{(A_d \Delta f)^{1/2}}{NEP} \quad (13)$$

where NEP is the noise equivalent power and Δf is the bandwidth. As pointed out, the noise bandwidth of the measurement system is the Nyquist frequency ($1/2T_I$), 500 Hz, although the filter bandwidth is 1000 Hz. The noise equivalent power, NEP, is simply determined from the transfer function measurement shown in Figure 19 and, is equal to 2.4×10^{-14} watts. Using these values, we can determine that $D^* \text{ (measurement)} = 5.1 \times 10^{12}$ cm (Hz)^{1/2}/watt.

The theoretical expression for $D^* \text{ (BLIP)}$, the background-limited performance, is derived from the shot noise of the background photon flux density⁽¹²⁾, Q_B , and is given by

$$D_{\lambda_0}^* \text{ (BLIP)} = \frac{\lambda_0}{hc} (\eta/2Q_B)^{1/2}, \quad (14)$$

where all of the quantities are well-known. For $Q_B = 4.2 \times 10^{12}$ photons/sec-cm² and $\lambda_0 = 4.18 \mu\text{m}$, the $D_{\lambda_0}^* \text{ (BLIP)}$ is equal to 5.1×10^{12} cm(Hz)^{1/2}/watt, the same value obtained from the above-described measurement.

We have also measured the background shot noise at different background levels (see Figure 20). The number of rms noise carriers was plotted as a function of the carriers generated by the background photon flux. The straight line represents the theoretical relationship between the shot noise and the number of carriers. The noise voltage causes the rms voltmeter needle to swing back and forth. When we took our data, we waited for a few minutes at each data point. The circled points represent the average values of the meter readings and the bars on these points represent the typical spread of the readings. The number of rms noise carriers of this spread was in the range of 70 carriers and the spread tends to increase with higher carriers.

As shown in Figure 20, the experimental results are in good agreement with the theoretical values in the high-carrier region. In the low-carrier region, however, the measured number of rms noise carriers tends to saturate at about 200 carriers. It will be shown below that this noise is due to the additional contribution of the dark current shot noise. The two data points shown at a background level of high 10^{13} photons/sec-cm² were measured under background-simulated conditions. That is, equivalent background carriers were generated with a blackbody source (dc radiation) rather than a 300°K background photon flux. For this measurement we used a small cold aperture that yielded a flux of $Q_B(300^\circ\text{K}) = 10^{12}$ photons/sec-cm² (the lowest value used in our present experiment, as shown in Figure 20). The number of carriers generated by the blackbody source was much higher than that of the background (300°K), so that the generated carriers should be determined only with the known blackbody source radiation. As shown in Figure 20, the experimental data points fit the other data points and the theoretical line quite well.

As mentioned, in the low background region, $Q_B = 10^{12}$ photons/sec-cm², the number of rms noise carriers is about 200, but the theoretical value is about 120. For Eq. (7), thus, the measured total rms noise is

$$(200)^2 = N_{\text{amp}}^2 + N_{\text{DN}}^2 + (120)^2. \quad (15)$$

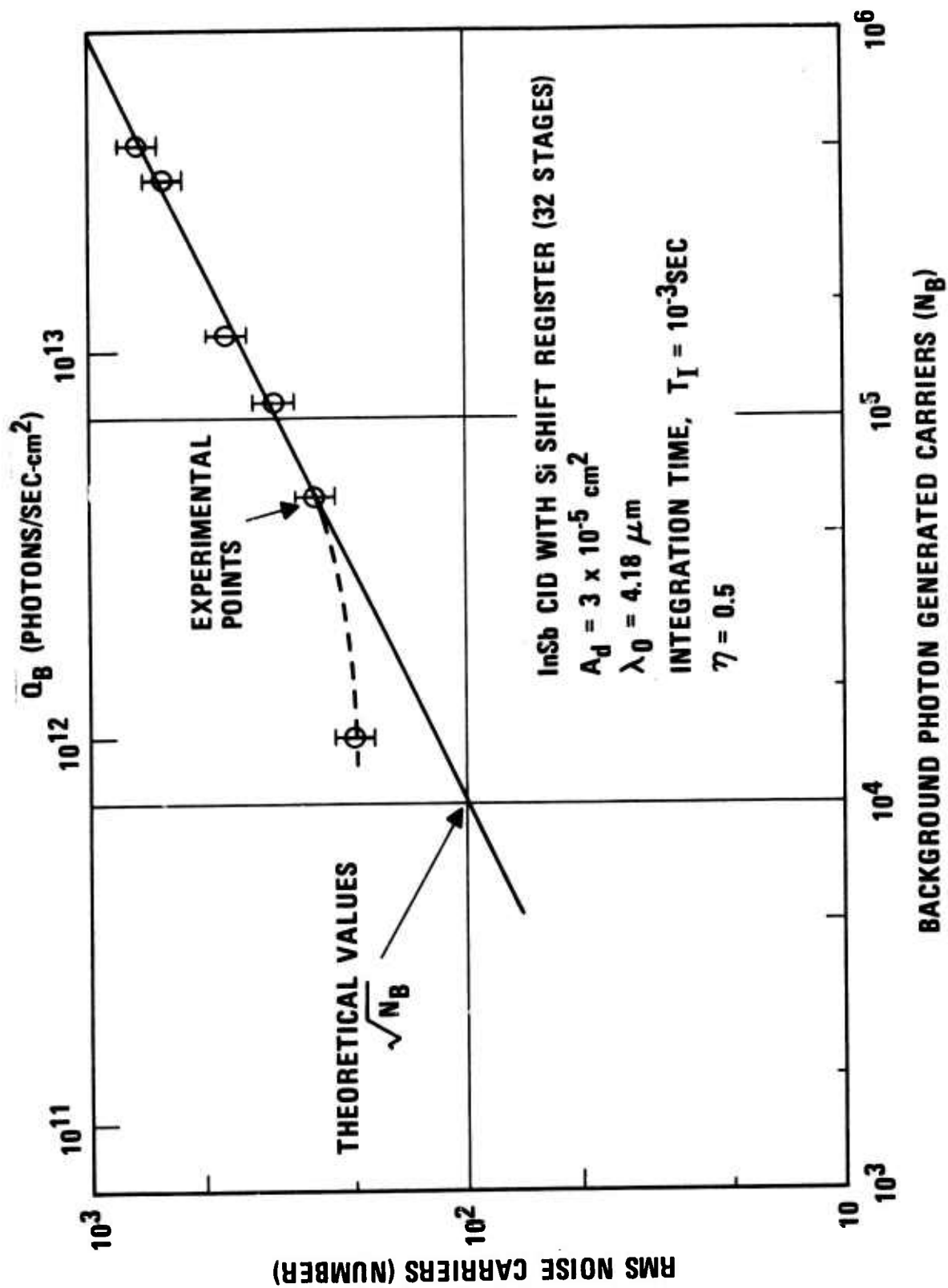


Figure 20. Measured Background Shot Noise Versus the Carriers Generated by the Background Photon Flux.

The InSb dark current shot noise and amplifier noise were measured together, see Eq. (9), by shielding the InSb devices from the background photon flux density; the number of these noise carriers was equal to 170. If we substitute this value in Eq. (15), the total number of carriers is equal to 210, which is very near the measured value of 200. Therefore, it appears that in the low background region ($Q_B \leq 10^{12}$ photons/sec-cm²) the amplifier and dark current shot noises dominate. Since the number of amplifier noise carriers is about 100, the number of dark current shot noise carriers (N_{DN}) is about 140; i.e. $(170)^2 = (100)^2 + N_{DN}^2$. The number of dark current carriers (N_D) is, thus, about 2×10^4 , which is equivalent to a current density of 10^{-7} amps/cm². This value is well within the range of the expected dark current density of InSb at 77°K.

V. FABRICATION OF InSb CID ARRAY

1. Array Mask Design

Figure 21 shows a design of a 1x16 one-column array. The 16 row bonding pads are arranged in an alternate pattern of left and right-hand sides so that two silicon shift register scanners can easily be wire bonded. The active unit cell size for one case is 3x3.6 mils with a center-to-center spacing of 4.3 mils; the other case is 2x2.3 mils on 3 mil centers. Although the array is a line array, the structure is completely two-dimensional and so requires a multi-layer metallization process. There are 17 processing steps needed to complete the array requiring nine mask sets.

For two-dimensional CID array operation, a major concern is the charge transfer between the row and column gates in each resolution element. We have already discussed (Section IV) the charge injection operation for linear arrays; for that matter, any good InSb MIS capacitor is capable of producing charge injection signals. In the two-dimensional case, however, charge injection and transfer must occur on the basis of element selection. That is, for the selected element, charge injection takes place while the charge on unselected elements is transferred to avoid charge injection. Only charge injection yields a video signal. The charge transfer operation between the row and column gates in the unit cell can be accomplished by using an overlapped electrode structure or a diffused island bridging the row and column electrodes. The overlapped gate configuration is used in the present one-column array design.

For the array design shown in Figure 21, the overlapped region is 0.2 mils. The active area of the row gates is half that of the column gates, but the row gate oxide thickness is half that of the column gate thickness, so the capacitance of two respective gates is equal, resulting in an equal charge storage capacity.

InSb CID ARRAY (1x16)

ACTIVE CELL SIZE = 3×3.6 MILS

CENTER-TO-CENTER SPACING = 4.3 MILS

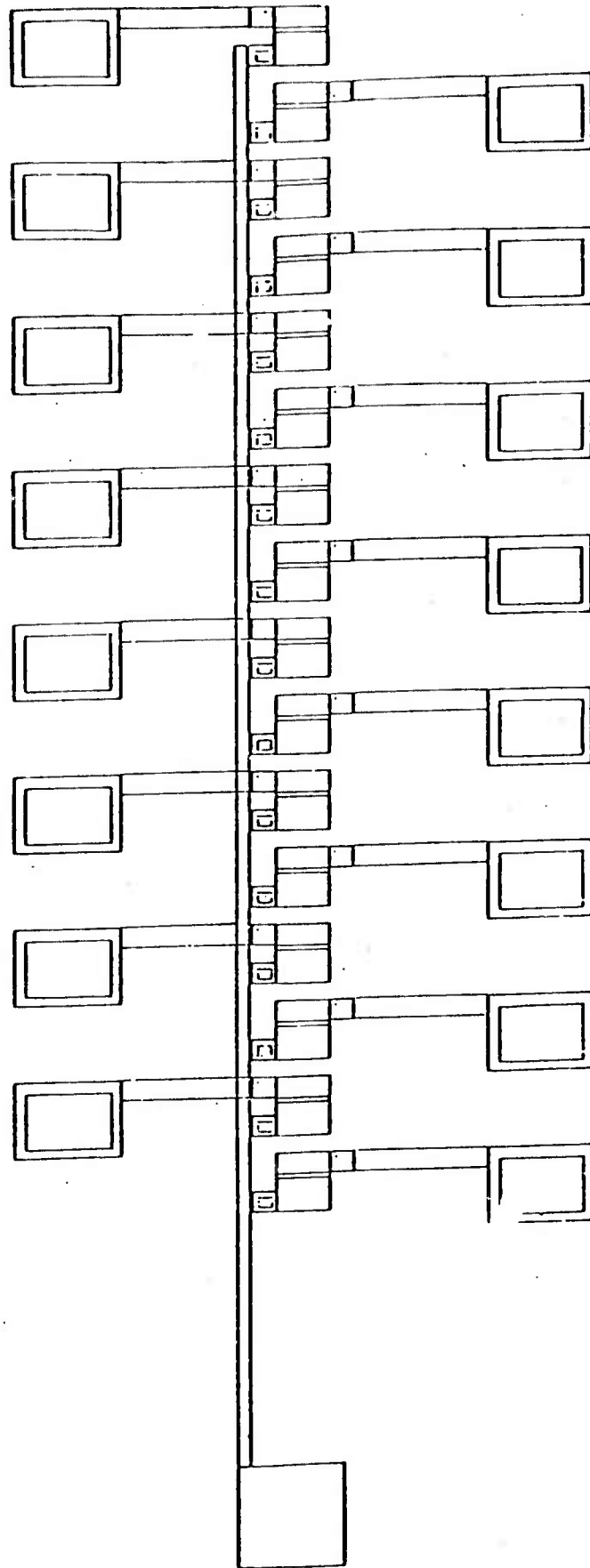


Figure 21. Design of 1x16 InSb CID Array for One-Column Area Array, Showing 16 Row Elements with Alternate Bonding Pads.

2. InSb CID Array Fabrication

Since the array structure requires a multi-layer metallization process with accurately resolved geometries, state-of-the-art photolithographic and wet-chemistry techniques are used to fabricate the array. Our initial concern was that the photoresist and chemical etchants might degrade the MIS interface properties, but the experimental results showed that this was not the case. There was no sign of device degradation after the wet-chemical process and the photolithographic technique routinely resolves 0.4 mil line widths of photoetched patterns on InSb MIS structure.

The SiON dielectric layers were used for both the gate and field oxides and for the multi-layer metallization process. For gate oxide thickness control, we first deposit a relatively thick oxide and then etch back to the desired thickness. We have been able to precisely control the etching rate of the SiON oxide layer and to etch down to a few hundred Angstroms. For the multi-layer process, the SiON layer is employed as an overlay oxide. After the first steps of the array process (e.g., the photoresist and wet chemistry processes), a second SiON layer is deposited over the processed array and the initial steps are repeated. This overlay oxide technique is also used for the thick-field oxide application. That is, after depositing the initial thin gate oxide and forming active gate sites, a thick-field oxide is deposited over the processed array for the lead interconnection patterns.

For the array metallization process, we usually use semi-transparent NiCr for the active region gate, and NiCr-Au for the lead interconnections in the thick-oxide region. We have also used semi-transparent Ti as the gate electrode, and obtained equally good MIS device characteristics. However, the NiCr electrode is somewhat easier to process than the Ti, and we now use NiCr exclusively.

For the field oxide, we use thick SiON dielectric layers. In the array structure, the metal leads on the field oxide must not create a potential well beneath the lead pattern. We have studied 20 mil-diameter MIS structures as a function of the thickness of the SiON dielectric layer.

The flatband voltage increases in the negative bias direction as the oxide thickness increases; for a thickness of about 7000\AA , the flatband voltage was in the range of -20 volts. However, the bias voltage is normally less than -10 volts and, thus, the -20 volt value seems more than adequate. We have also fabricated thin oxide MIS structures by etching the deposited thick SiON layer; the resultant flatband voltage was decreased to about -5 volts. These results, therefore, suggest that the flatband voltage of the MIS structure of SiON is controlled by the built-in oxide charges, normally observed in SiO_2 on Si MIS structures. In the InSb CID array fabrication process, therefore, the thickness of the SiON layer plays an important role.

Better controlled field oxide experiments have been performed. We have accurately etched the initial oxide down to 6000\AA , 4000\AA , and 2000\AA , respectively. Narrow and long lead patterns (0.8×45 mils or 0.8×60 mils) of metal gates were made using a photoresist technique and the C-V characteristics of the finished structures were measured as a function of oxide thickness. The results are shown in Figure 22. The 2000\AA thick oxide reveals a normal C-V curve, but the thick oxide MIS structure showed no MIS C-V characteristic, suggesting that the latter cannot create potential wells beneath the metal. It appears, therefore, that the field oxide thickness must be greater than 4000\AA to minimize cross-talk among the resolution elements in the array.

The effect of the relative oxide thickness was investigated using two sets of thicknesses:

	<u>Type A</u>	<u>Type B</u>
Row gates oxide thickness:	1800\AA	900\AA
Column gates oxide thickness:	2700\AA	1400\AA
Row gates field oxide thickness:	6600\AA	2700\AA
Column gates field oxide thickness:	8000\AA	5200\AA

The Type A arrays showed acceptable C-V curves for the row gates, but the depletion depth of the column gate was too small. In some cases, oxide cracking or peeling was observed. The Type B arrays, on the other hand, with a total oxide layer thickness of 6000\AA , showed no cracking. This array showed somewhat inconsistent row gate C-V data, and the column gate

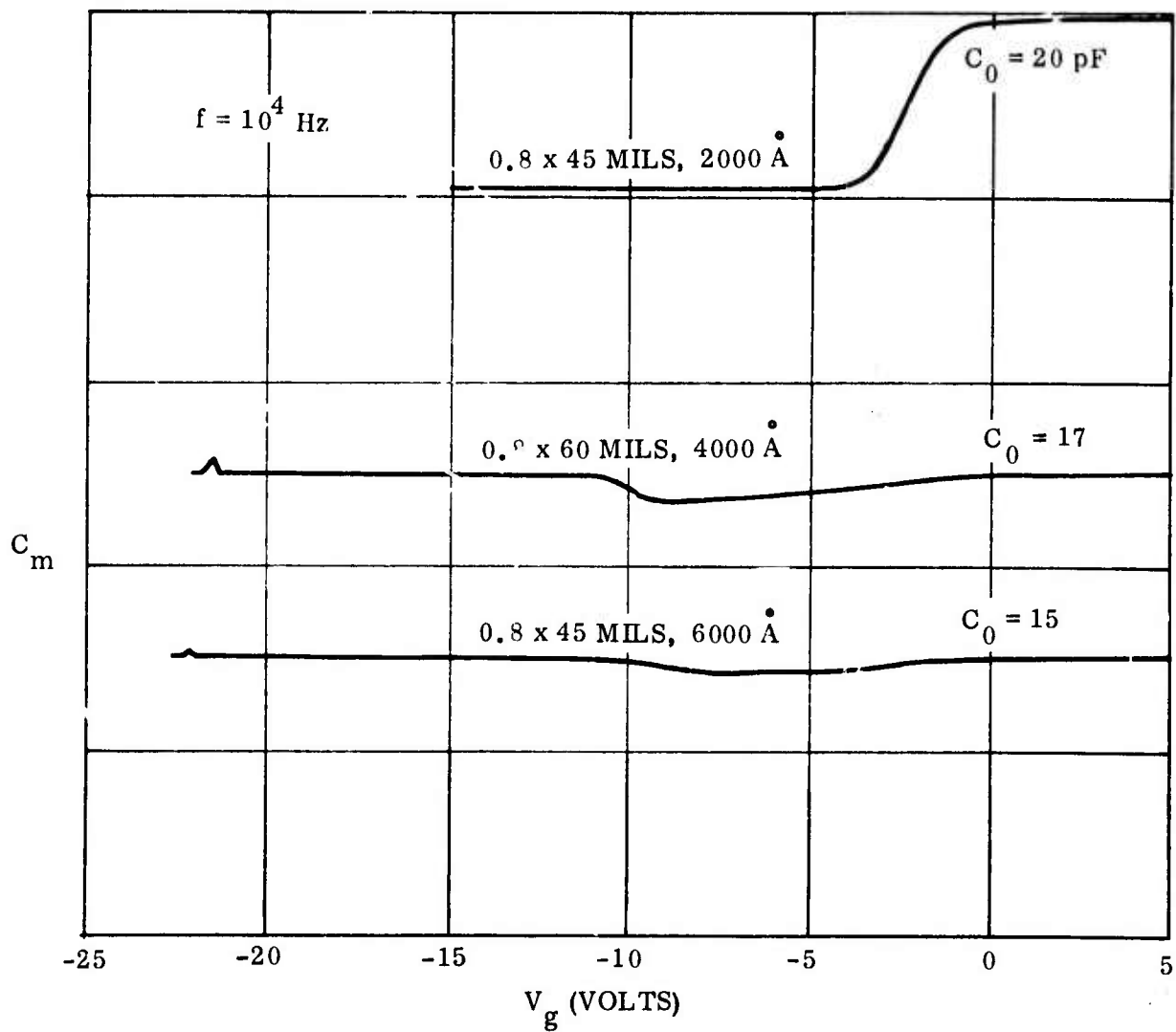


Figure 22. C-V Characteristics of Long Lead Pattern InSb MIS Structures.

had a normal C-V characteristic. One explanation is that the row gate field oxide is too thin and so, the row gate contact leads create a depletion region underneath the field oxide.

The C-V curves for a thin-oxide array are shown in Figure 23; the upper curve represents the column gate and the lower five C-V curves are for the five row gates, respectively. Note that the small bumps shown in the inversion bias region appear to be due to the creation of a depletion region under the lead pattern on the relatively thin field oxide. The row gate field oxide thickness for this array was about 3300\AA and the thickness of the column gate field oxide was 6200\AA . Thus, the effect of the bump on the column gate C-V data is small.

For an array fabricated with a thick field oxide, such as a row gate field oxide thickness of 5000\AA and a column gate field oxide thickness of about 7000\AA , the perturbation in the C-V curve disappears and normal MIS characteristics are obtained, as shown in Figure 24. We conclude that the field oxide thickness must be greater than 5000\AA .

Since the thick oxide tends to peel from the wafer substrate (due to mechanical strain), we thinned the gate oxide to produce a larger ratio of gate to field oxide thickness. Up to about 500\AA , there seems to be no shorting and a strong indication that the gate oxide could be even thinner. In subsequent array processes, the row gate oxide thickness was varied from 500\AA to about 700\AA and the column gate was about 1300\AA .

Seventeen processing steps and nine photoresist mask sets are required for a complete array process. These steps are:

1. Deposition of thick SiON layer on InSb wafers
2. Etching down to form gate oxide (mask #1)
3. Metallization of row sensors and contact metal leads
4. Pattern the row contact metal leads (mask #2)
5. Pattern the row sensor gates (mask #3)
6. Deposit the overlap SiON layer between the row and column gates
7. Metallization of the column sensors and contact metal leads

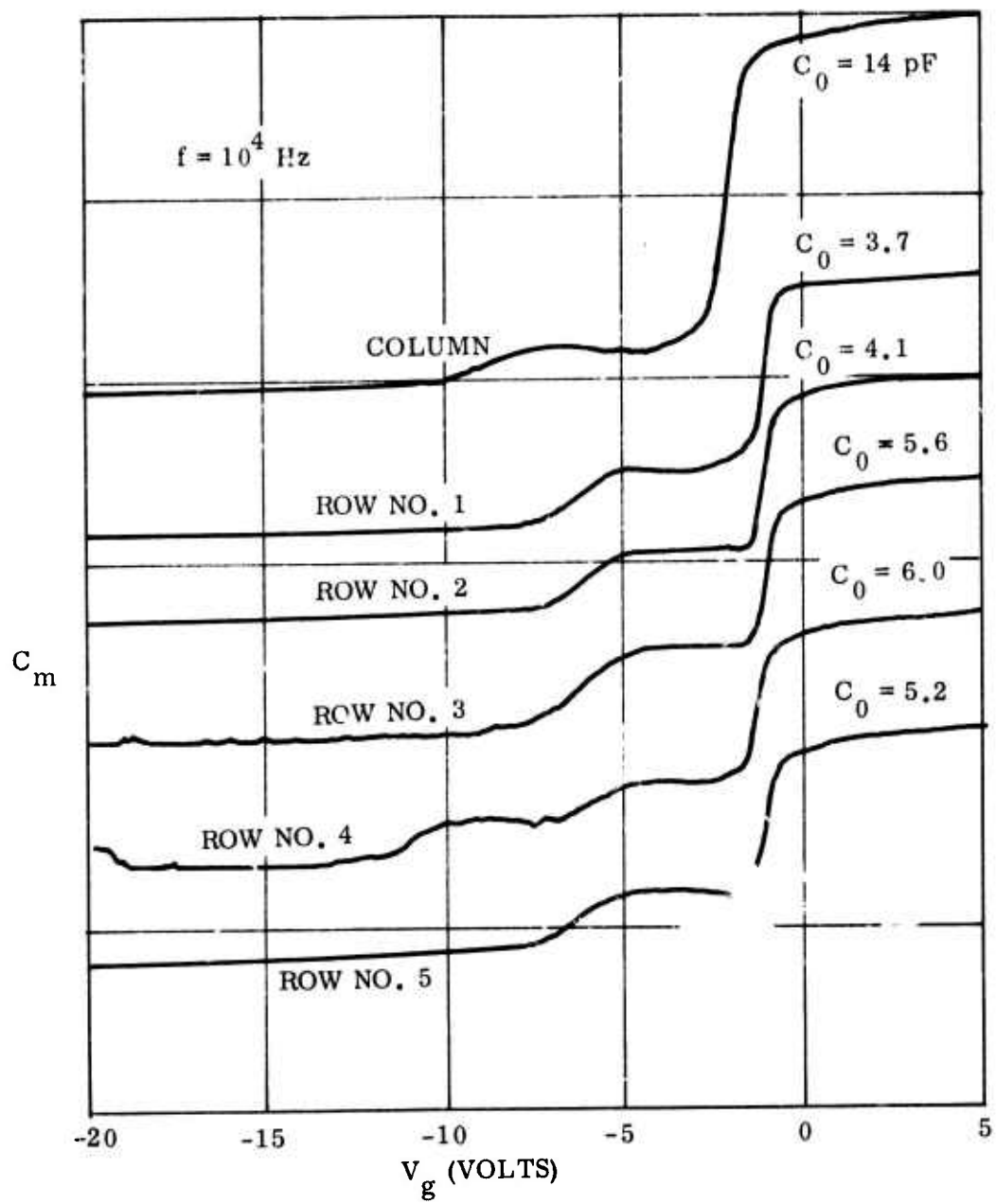


Figure 23. C-V Data for 1x16 InSb CID Array with Thin-Field Oxide.

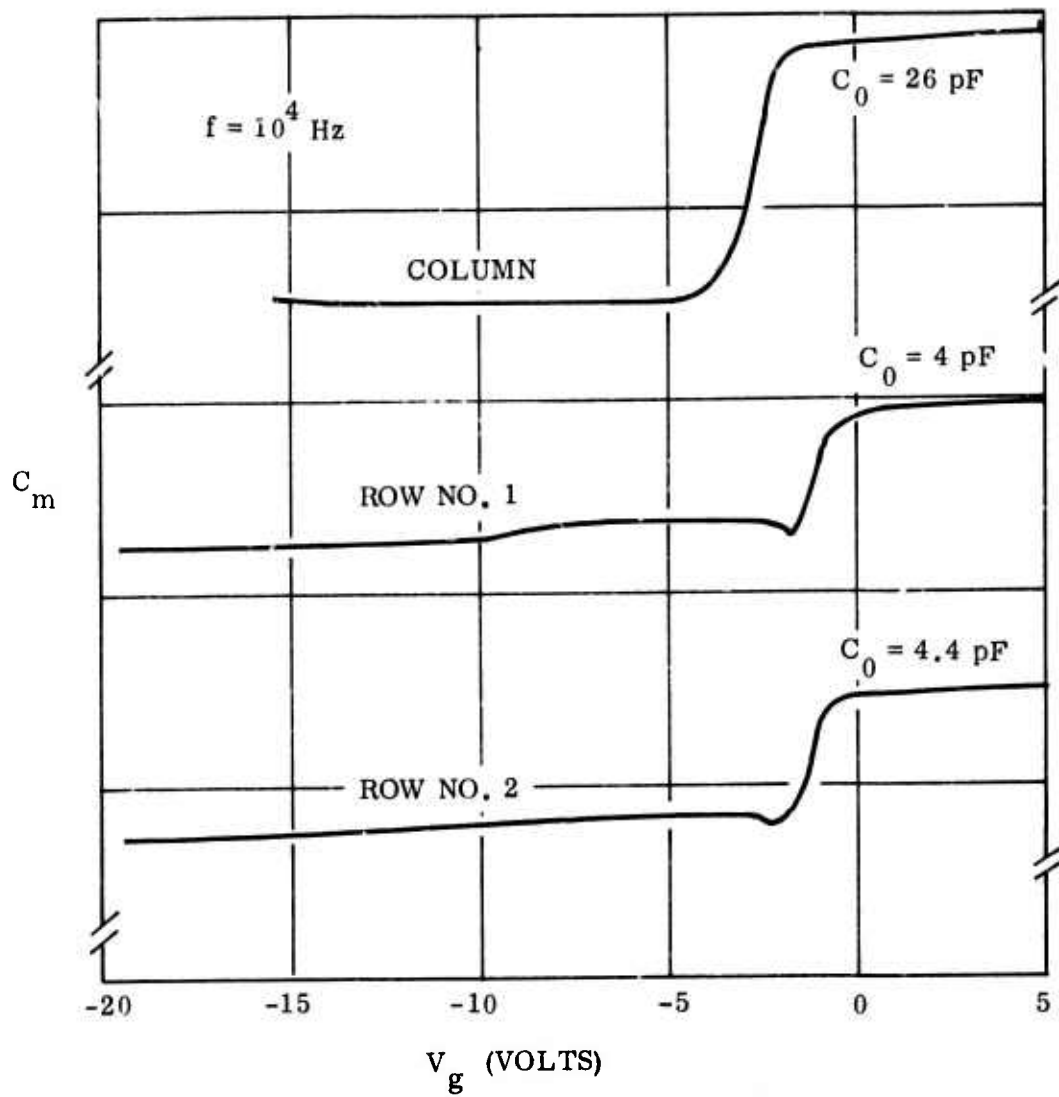


Figure 24. C-V Data for 1x16 InSb CID Array Having Thick-Field Oxide.

8. Pattern the column contact metal leads (mask #4)
9. Pattern the column sensor gates (mask #5)
10. Deposition of column protective SiON layer
11. Opening the row contact windows (mask #6)
12. Metallization of the row lead bonding pads
13. Pattern the row lead bonding pads (mask #7)
14. Deposition of a crossover SiON layer between the row and column metal leads
15. Opening of column contact windows (mask #8)
16. Metallization of column lead bonding pads
17. Pattern the column lead bonding pads (mask #9)

The key processing steps are briefly discussed below.

- A. All photoresist processes are the same. Kodak Negative Resist is spun on the wafers at about 4000 RPM for 20 secs. The wafers are pre-cured for one-half hour at 85°C in a N₂ ambient, exposed on a standard aligner, developed with Kodak developer, rinsed, dried by spinning and then post-cured for one hour at 145°C in a N₂ ambient.
- B. All SiON oxides are etched in a 4% HF solution.
- C. All metallizations are Nichrome followed sequentially by evaporating gold in 5x10⁻⁷ torr at a substrate temperature of about 150°C.
- D. All dielectric layers used in the array fabrication are SiON. The deposition technique has been discussed in Section II.
- E. All Nichrome etchings were done with a 1:1 ratio of HCl and N₂O at 50°C, and the gold was etched with a solution of KI.
- F. All photoresist patterns, after usage, are removed with a microstrip set at 100°C.
- G. After each wet-chemical process, the wafers were cleaned thoroughly with DI water.

Figure 25 shows a typical photograph of a completely processed 1x16 array fabricated in accordance with the above processing steps.

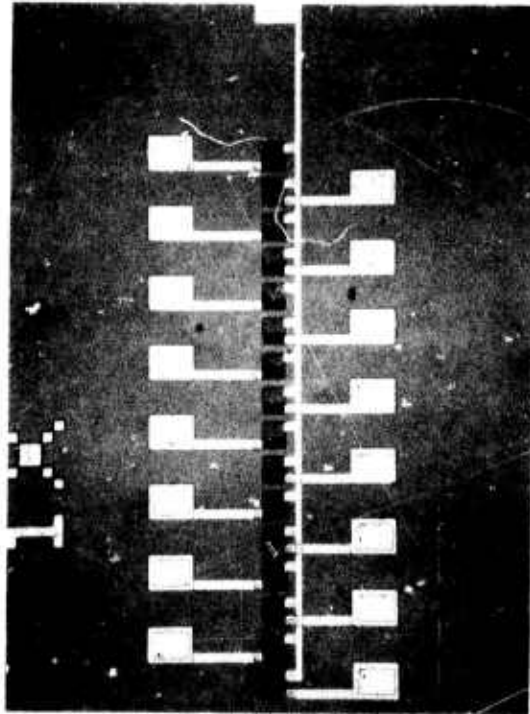


Figure 25. Photograph of Completely Processed 1x16 InSb CID Array.

For the initial evaluation, we used a simple room temperature probe to test the arrays in the wafer, measuring the oxide capacitance in the row elements and the common column gate. If there is any shorted or open element in the array, no further test is made. The arrays that passed the initial mechanical test were further evaluated at 77°K. For this, we mounted the arrays in special array packages, as discussed below.

3. Array Package and Interconnection

A complete array package is shown in Figure 26. Twenty lead ceramic flatpack packages were used for this work. As pointed out, the array bonding pads were arranged so that two silicon scanners can be used for easy wire bonding. Common input pulses were used to drive the silicon scanners, but all the odd-numbered output stages (for the left-hand side scanner) were used and all the even-numbered output stages (for right-hand side scanner) were connected so that all the array elements could be read in sequence.

Inside, the ceramic package was metallized with nichrome/gold to make a common ground plane. Two ceramic bonding strips were employed to bridge the bonding between the silicon scanner and the InSb array. These strips were made separately via photoresist patterns. Matched pairs of silicon shift registers and two bonding strips were mounted with (Epotek H-31) single component conductive epoxy and then cured at about 150°C for 30 minutes. The silicon scanners were ultrasonically bonded to the package leads and the bonding strips, and the package was tested by operating the scanners. The two output test points of the scanners were used to monitor the scanner operation. The InSb array chip was epoxied, as before, after the scanners were evaluated. The InSb array chip was centered between the bonding strips and thermocompression bonder was used with a small indium ball between the bonding pan and gold wire.

Each silicon scanner has a MOSFET device with a reset switch transistor that can be used as a preamplifier inside the dewar. For the array interconnection the 16 row elements are connected to the silicon scanner output stages; the common column line is tied to a preamplifier transistor

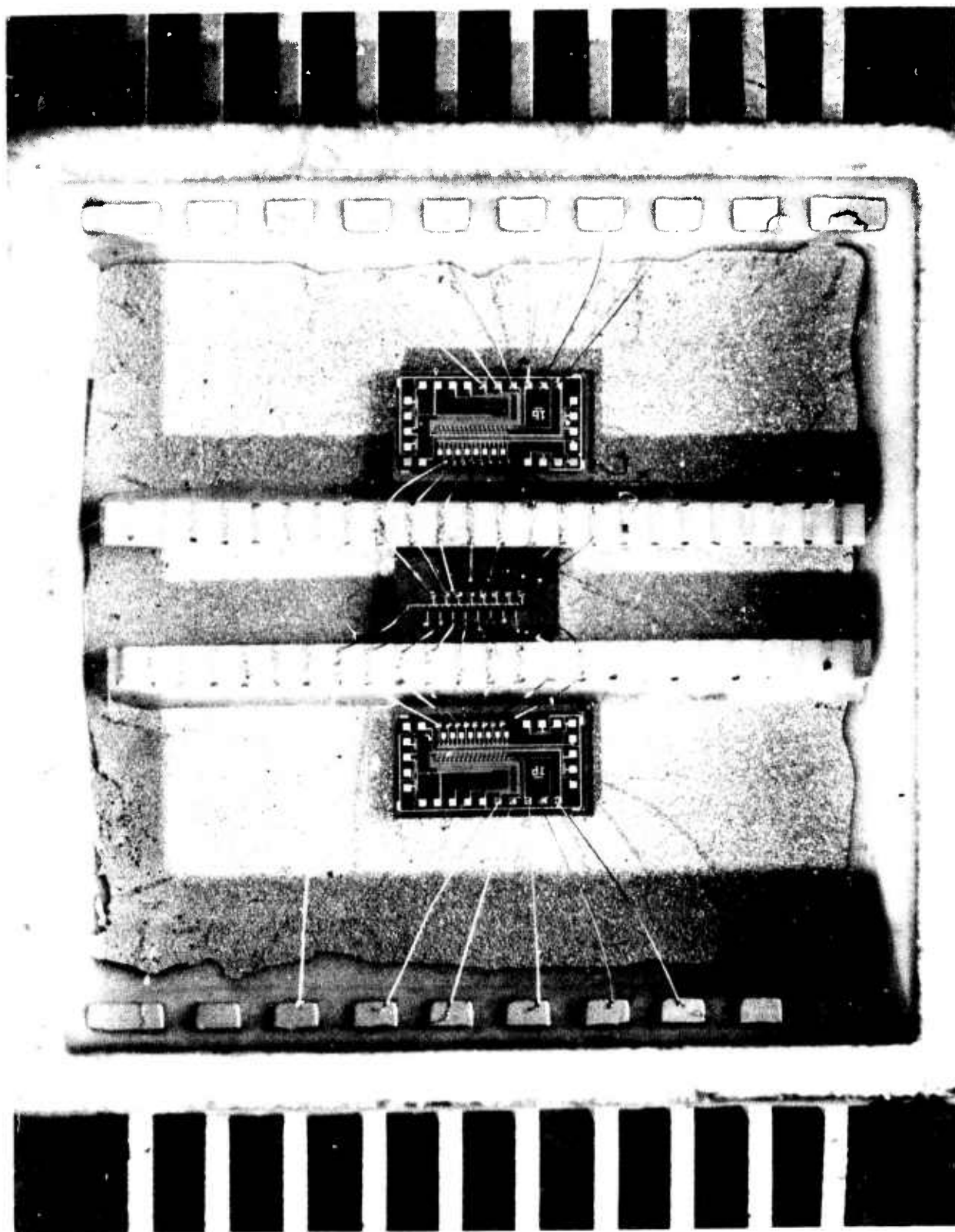


Figure 26. Photograph of Packaged 1x16 InSb CTD Array with Two Si Scanners.

gate, an injection coupling capacitance and a reset switch. The injection coupling capacitance was used inside the dewar with the array package. Additional MOSFET switches provided for the row gate bias. After packaging and interconnection, the arrays are ready to be evaluated at 77°K.

VI. SILICON SCANNER DESIGN, FABRICATION, AND OPERATION*

1. Introduction

Imaging arrays utilizing the CID principle require a mechanization for selecting a row and column lines. This could be done by use of two shift registers. However, since every line (row or column) need be addressed just once during a scan, only one logic level "one" is needed in each register. Since a signal "one" is always trailed by a series of logic "zero" levels, we really require a scanner instead of a shift register.

For this reason, we can simplify the design of the scanner if we allow that each step of the scanner will be set to a logic level "zero" following a logic level "one". Furthermore, by designing this scanner with non-inverting stages, the number of parallel output doubles in comparison to a conventional register made with inverting stage. In the conventional register, the output can be tapped only once for every pair of inverters because the signal and its complement must be held in every stage.

A main concern in the design of a scanner is the regeneration of the signal at every stage for compensating the signal losses in the transfers, particularly those due to gate threshold drops. This problem is overcome with the introduction of bootstrapping in the form of a MOSVAC capacitor, which has the desirable property of being active only in the presence of a signal "one". This signal regeneration mechanism is inserted at each stage as the signal is transmitted only if the signal is above the gate threshold value and thereby providing a main rejection mechanism.

This scanner is clocked by two-phase lines with the clock pulses alternatively fed to one or the other. At any time there is a phase line at ground level acting as the return for the other phase line. No separate ground bus is required.

*This scanner was invented and developed by J.L. Mundy, R.E. Joynson, H.K. Burke, G.J. Michon and M. Ghezzi of the General Electric Corporate Research & Development Center. This work is about to be published and is covered by U.S. Patent 3,808,458.

2. Circuit Description

This section describes the basic circuit configuration of the scanner while the operation will be described in the next section. Four MOS transistors are active elements of each stage, as shown in Figure 27. Two of them T_1 and T_3 have large aspect ratios in order to transfer the phase line clock pulse to the output tap (C_2) and to precharge the next MOSVAC (T_8) with the smallest possible delay. The gate of T_1 is connected to the gate of the bootstrapped MOS capacitor T_4 , which can rise above the phase line voltage and transfer at high speed without threshold losses. For achieving a significant bootstrapping action, the combined gate capacitance of T_4 and T_1 should be large. As the design of T_1 is largely dictated by the selection of an appropriate transconductance value, the main bootstrapping capacitance is provided by T_4 , which is laid out as a large area device with aspect ratio close to one and with source and drain tied together. As T_4 acts like a charge reservoir, the square geometry provides an optimum charge access to the output port allowing shorter time delays in charging and discharging.

Transistor T_3 is connected in a diode configuration with the gate and the drain tied together. As a result it allows the charging of node 5 to take place, but it cuts off the discharge path, electrically isolating this node during the falloff of the phase pulse ϕ_1 .

Finally, transistor T_2 provides a discharge path for the bootstrapping capacitance bringing the gate voltage of T_4 and T_1 to ground after the charging of node 5 has taken place. This transistor should be designed with minimum geometry, because it is turned on after node 5 has been electrically isolated during the falloff of the phase pulse ϕ_1 and therefore reduces the bootstrapping action of T_8 by coupling node 5 to ground.

The aspect ratio of transistor T_2 should also be small in comparison to that of T_1 for assuring that T_1 completes the discharge of node 4 before it is turned off by the simultaneous discharge of node 3 through T_2 .

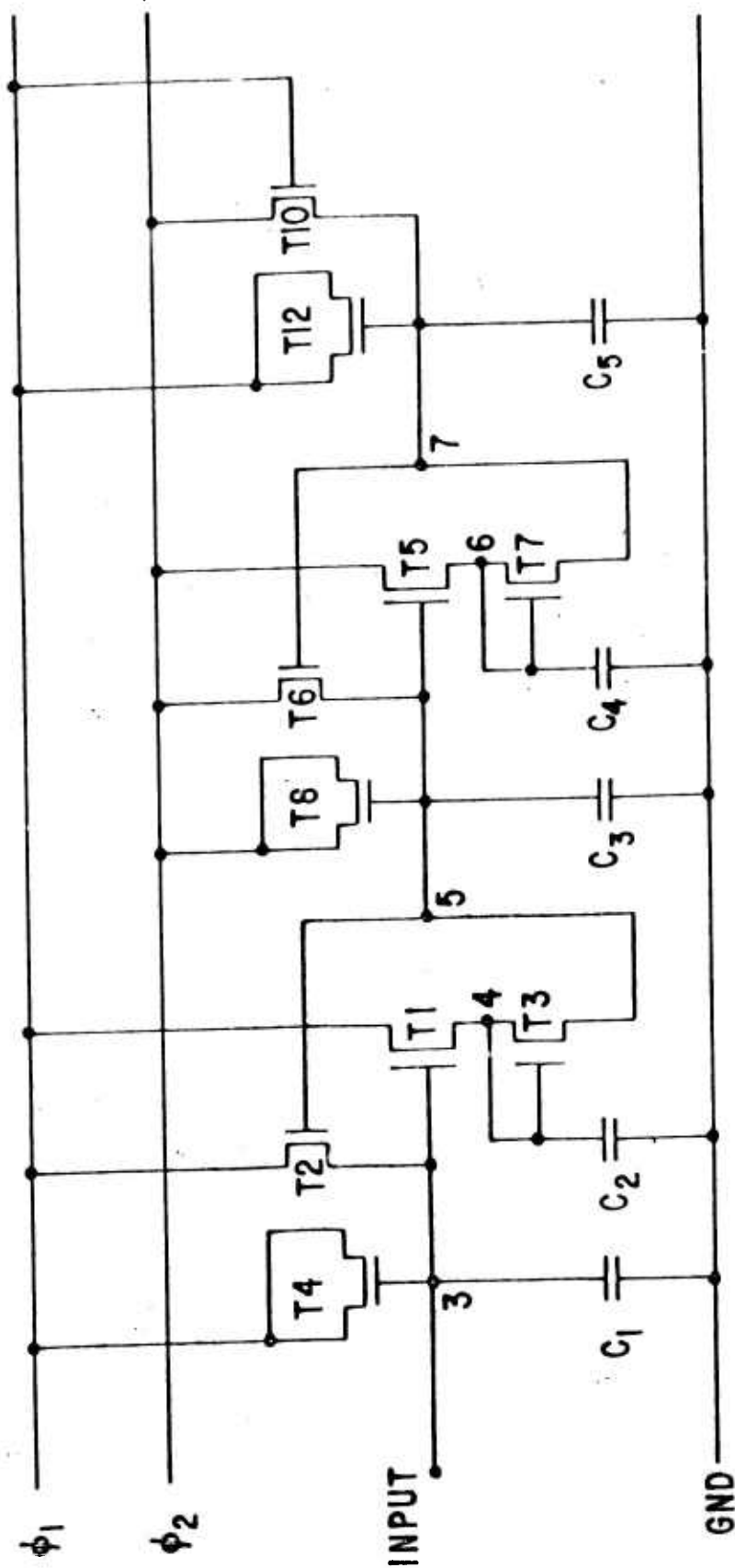


Figure 27. Scanner circuit diagram.

3. Scanner Operation

As we refer to p-channel devices, let us consider that in the initial condition the input voltage V_3 is negative and equal to V_0 which is equivalent to a logic level "one". As a result, transistor T_4 is "on" determining a strong capacitive coupling between the input and the phase line ϕ_1 . This coupling is due to the formation of an inversion layer beneath the gate of T_4 , which can be interpreted as an extension of the source and drain regions in the computation of the gate-source (drain) capacitance.

As the phase line ϕ_1 is pulsed from 0 to V_ϕ , the large capacitance of T_4 overrides the capacitance to ground C_1 and bootstraps V_3 to V_{BS} which must be larger than V_ϕ for a complete transmission of pulse ϕ_1 through transistor T_1 without threshold losses. The harder T_1 is turned "on", the shorter is the lag in the rise time of pulse ϕ_1 at node 4. Transistor T_3 is connected in a diode equivalent configuration between nodes 4 and 5 and is "on" when V_4 is more negative than V_5 by at least a threshold voltage, V_T .

Thus under the influence of pulse ϕ_1 transistor T_3 conducts and draws current from node 4 for charging C_3 and the gate to source (drain) capacitances of T_5 and T_8 . It will eventually stop conduction when V_3 equals $(V_\phi - V_T)$, assuming that the gate of T_3 is at V_ϕ .

Transistor T_2 is turned off during the ϕ_1 pulse, because even when the gate is at the peak voltage $(V_\phi - V_T)$, this voltage is still less than the source and drain voltages, V_ϕ and V_{BS} respectively. Thus any current drain is precluded from node 3, and the bootstrap voltage remains constantly applied to the gate of T_1 until the pulse ends.

When the phase line ϕ_1 falls back to zero, transistor T_3 is turned off immediately, letting the voltage at node 5 to reach its equilibrium value V_0 as a result of charge redistribution between C_3 and the capacitances of transistors T_2 , T_5 , T_8 , and in smaller degree of T_3 . Simultaneously, V_3 is brought back to its initial voltage, V_0 , as the boot-

strapping action of T_4 now occurs in reverse, and from this level V_3 falls rapidly to zero as the charge at node 3 drains through T_2 , which is now "on".

The voltage at node 4, V_4 , is also decreasing rapidly to zero as C_2 and the capacitance of T_3 are discharged through transistor T_1 to phase ϕ_1 , which is now zero. Caution must be exercised in the scanner design to ensure that V_3 does not fall to zero faster than V_4 , because as soon as V_3 is within a threshold drop from ϕ_1 , T_1 is turned "off" freezing the residual voltage V_4 . This problem is avoided by choosing a much larger aspect ratio for T_1 than for T_2 and by keeping the capacitance C_2 reasonably small.

When the phase pulse ϕ_2 starts, the bootstrapping action raises V_s from V_0 to V_{BS} , repeating the cycle already described for V_3 and pulse ϕ_1 .

For completeness, let us consider the case where in the initial condition V_3 is below threshold, corresponding to a logic level "zero". As transistor T_4 is then turned "off", the bootstrapping action does not occur in presence of pulse ϕ_1 and coupling between node 3 and ground through C_1 prevails in keeping V_3 below threshold so as transistor T_1 remains "off" and no voltage change occurs in the following stages of the scanner.

In the circuit diagram, a convenient termination of the scanner is presented using transistor T_{10} with the source connected to phase ϕ_2 and the gate to phase ϕ_1 . This termination is aimed at preventing voltage disturbances generated by phase line couplings to the internal nodes from being reflected backward in the scanner altering the correct output. The following operational description applies to this termination. When ϕ_2 is on, V_7 is negative and T_{10} is "off", because its gate is zero, and it is tied to ϕ_1 . When both ϕ_2 and ϕ_1 are off, T_{10} still does not conduct because its gate is at source voltage and not a threshold below, as required for conduction. Only when ϕ_1 is on, T_{10} conducts and drains to zero the charge on T_{12} , if node 7 is at logic level "one". Thus the pulse on V_7 is shorter than the corresponding V_5 pulse because its terminal portion at voltage V_{BS} is reduced to merely a spike.

Examining the timing diagram, Figure 28, we observe the existence of two types of pulses, which can be used as outputs on a capacitive load -- for example, the gate of a decoder transistor. This feature adds considerable flexibility to this scanner, because in some applications it is preferable to have output pulses at adjacent locations which are slightly overlapping in time, like V_3 , V_5 , and V_7 , while in other cases a complete extinction of a pulse is required before the next pulse starts at the following output, like V_4 and V_6 . It is remarkable that these different types of pulses result from choosing different tapping locations in the scanner without any modification of the phase line pulses.

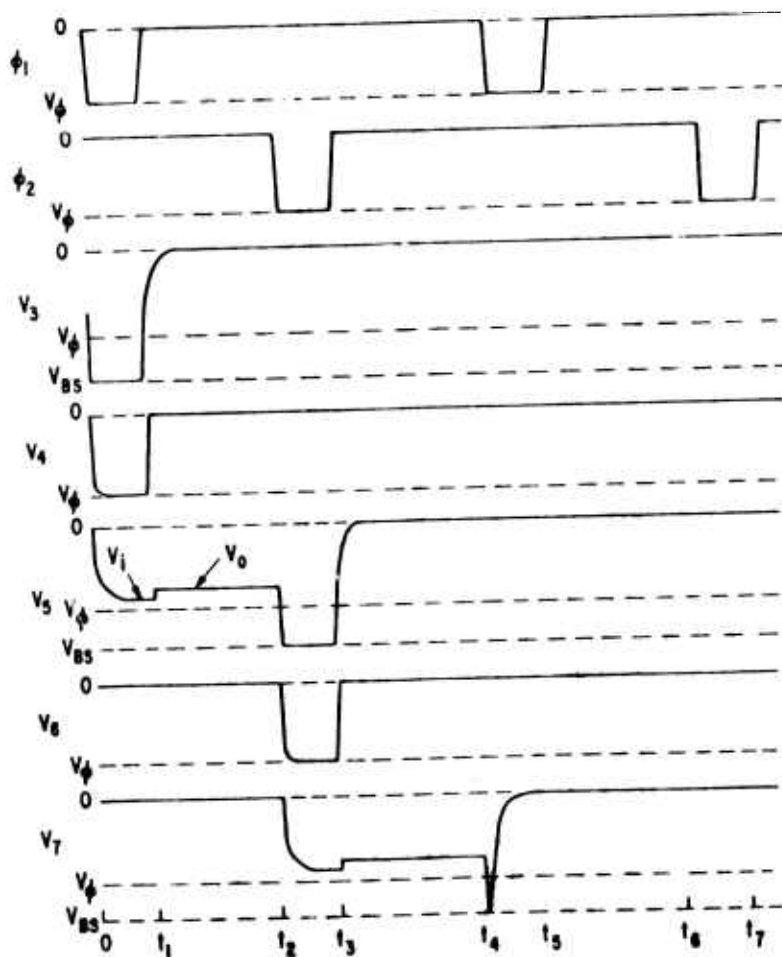


Figure 28. Scanner timing diagram.

The operation of the scanner has been investigated by G. J. Michon, H. K. Burke and M. Ghezze of the General Electric Corporate Research and Development Center, both analytically and experimentally. The transient I-V characteristics of the MOS transistors were derived and were compared to those of a SCEPTRE simulation based on the same numerical parameters. Good agreement was found in all cases even if approximations had to be introduced in the solution of the differential equations representing the transient I-V MOS response. An experimental confirmation of the scanner operation was obtained from a test chip.

4. 16-Stage Scanner

For the NRL InSb program, a 16-stage scanner was designed, simulated, fabricated and evaluated. The 16 element scanner is shown in Figure 29. The scanner output taps were connected to the gate of the enable transistor which, when activated, connects the enable line to a bonding pad. The bonding pads are, in turn, bonded to the InSb array lines. The Si chip also contains a large MOS transistor which can be used as a preamp, and other MOS transistors which could be used as reset switches if desired. The mirror image of the scanner was also included on the mask set.

The scanner used the non-overlapping outputs which are spaced on 3 mil centers. The output pads of the scanner are staggered to ease the spacing requirements during wire bonding. Also included are MOS switches located between the output pads and the enable transistors. These have common gates and can be used to simultaneously set the potential of output pads.

The actual design of the scanner made use of the previously mentioned analysis and was verified by computer simulation. The simulation was done using the MOSTRAN transient analysis program developed by the General Electric Integrated Circuits Center. This dynamic simulation of the MOS circuitry involves the simultaneous solution of a set of non-linear differential equations which are the nodal current Kirchhoff's equations.

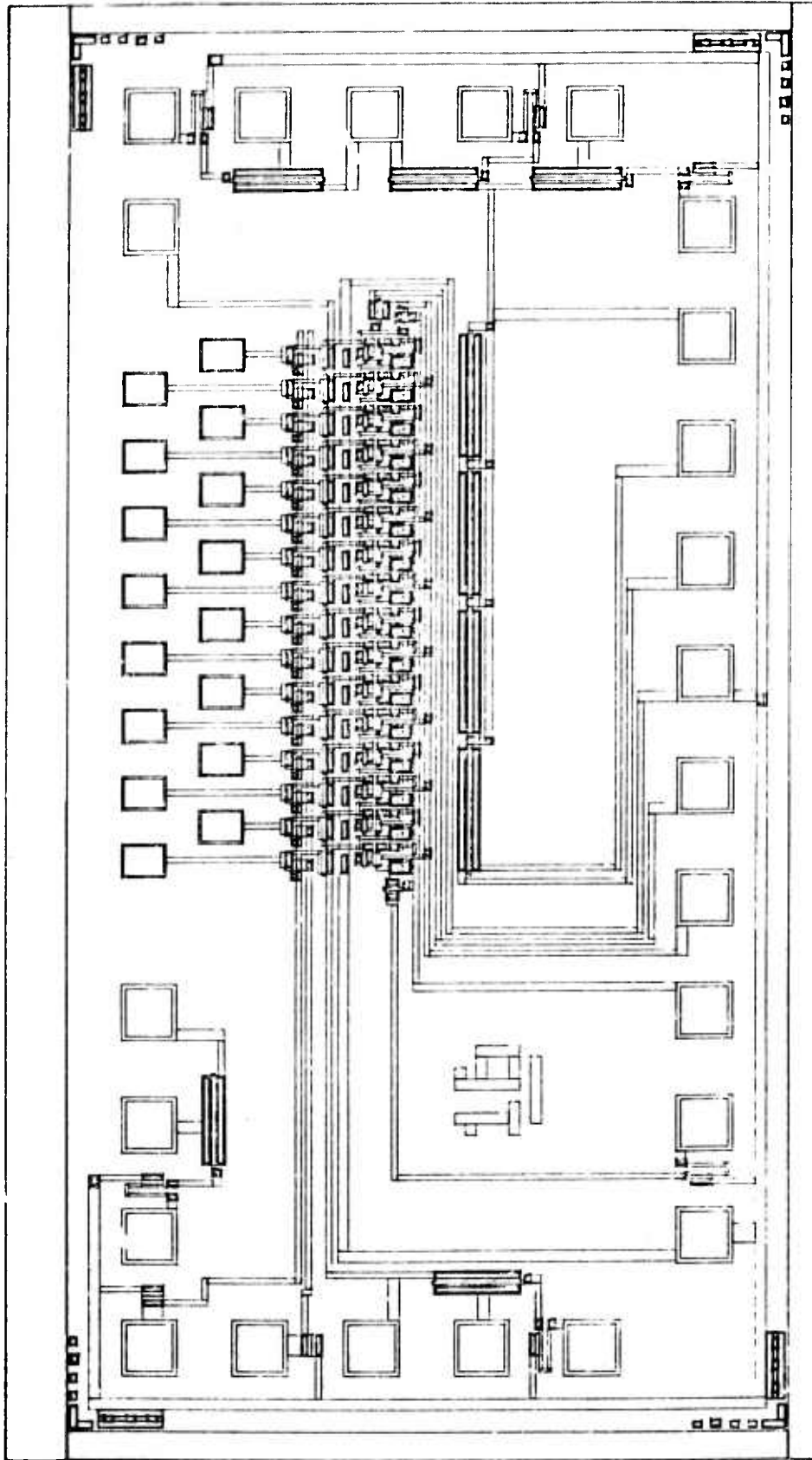


Figure 29. Layout of 16-Stage Silicon Scanner

This program uses the Sah equations⁽¹³⁾ for the MOS transistors and includes device geometries and process parameters. Also included were the parasitic capacitors for the actual layout used. The results of one such analysis is shown in Figure 30.

The circuit used for the simulation was for a scanning with 4 stages and included both the input and output termination circuits. The following parameters were used

Threshold voltage	- 1.0 volts
Gate oxide capacitance	- .186 pf/mil ²
Gate-source overlap	- .05 mils
K'	- 2.9 micromhos/volts ²
Φ_1 and Φ_2	- -12 volts

The results are as predicted from previous work. The non-overlapping output taps (nodes 4, 6, ...) follow the phase pulses fairly closely. The overlapping taps (nodes, 5, 7, ...) show the bootstrapping of the MOSVAC. It is expected that the scanner can be designed for 10 MHz operation.

The actual mask set was designed to include 16- and 32-stage shift register scanners and their mirror images. The scanners were then fabricated using the normal CID process. Figure 31 shows a photograph of completely processed silicon shift register scanner; it is a pair, the normal one and its mirror image.

After completing the fabrication process, the wafers were probe tested to select the working scanners (pairs) and then scribed into a chip for use with InSb array. The working scanner pairs were then mounted on a flatpack package and before connecting with an InSb array, the scanners were again further tested. The detailed identification of the bonding pads for the silicon scanner is shown in Figure 32 and the equivalent circuit is shown in Figure 33. For the initial scanner test, input, Φ_1 , Φ_2 , output, V_{GG} , V_{RB} , and enable line were connected and the output pulse was monitored for the operation.

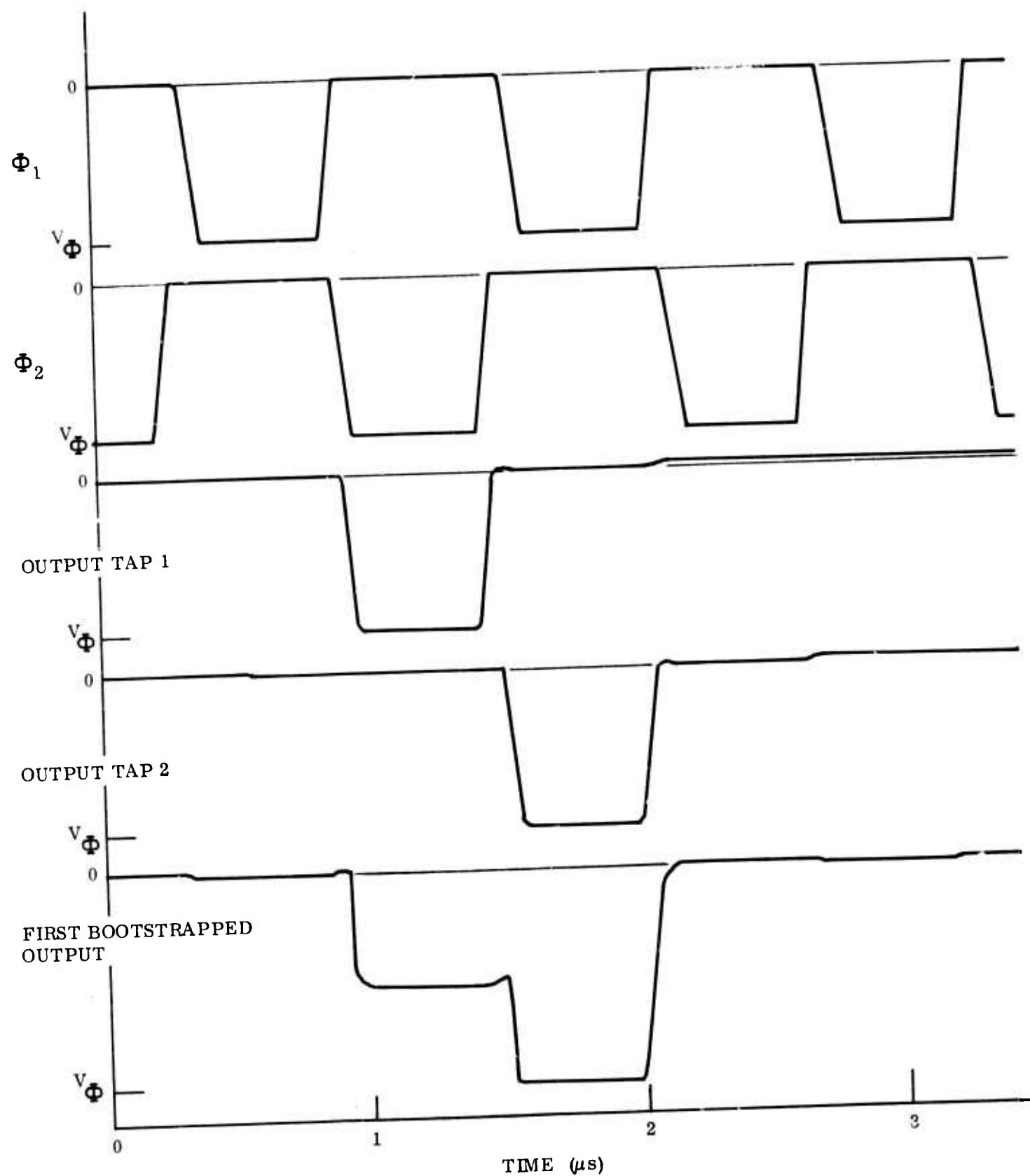


Figure 30. Results of Simulation of the Four Stage Si Scanner

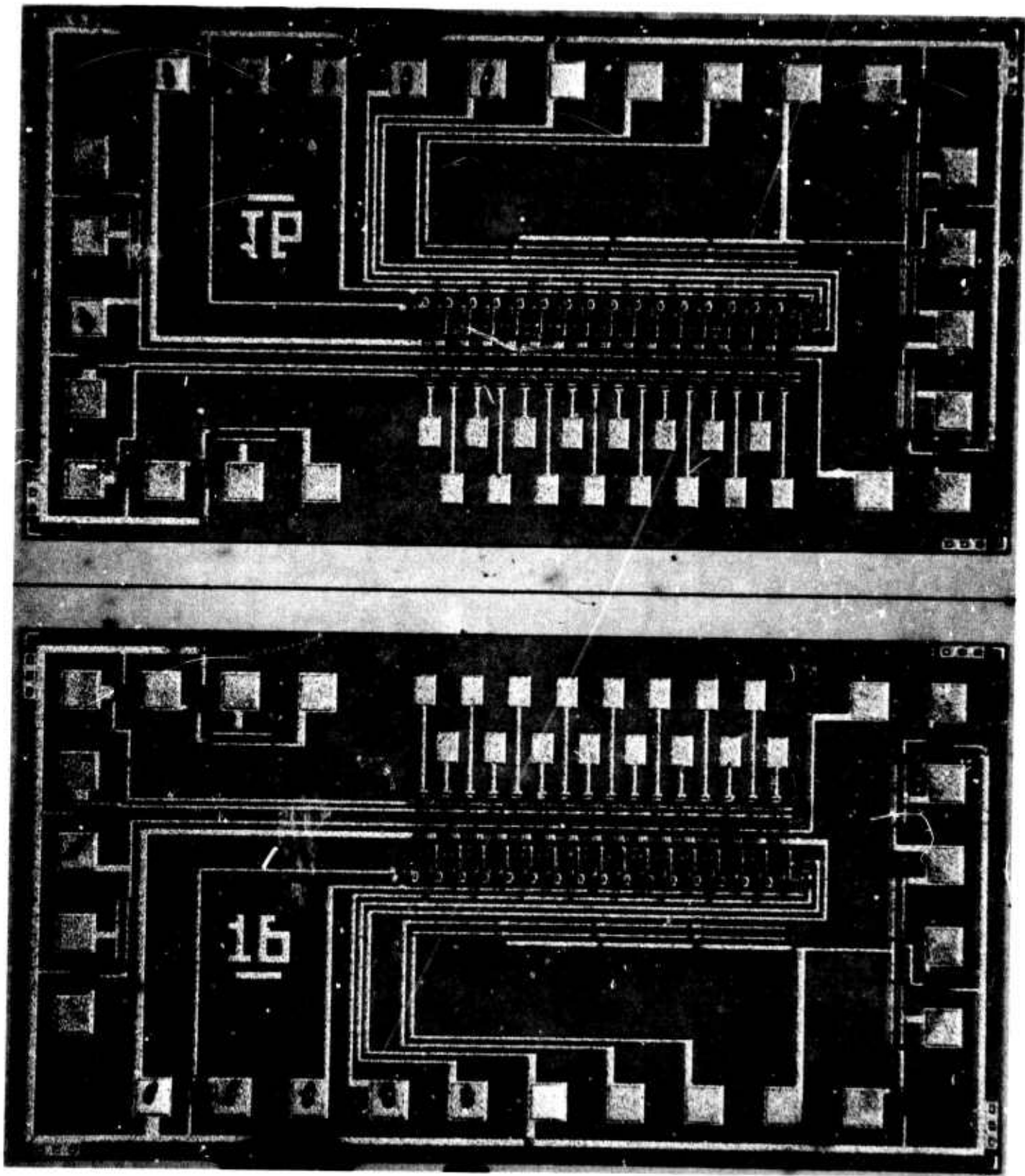


Figure 31. Photograph of 16-Stage Si Shift Register Scanners

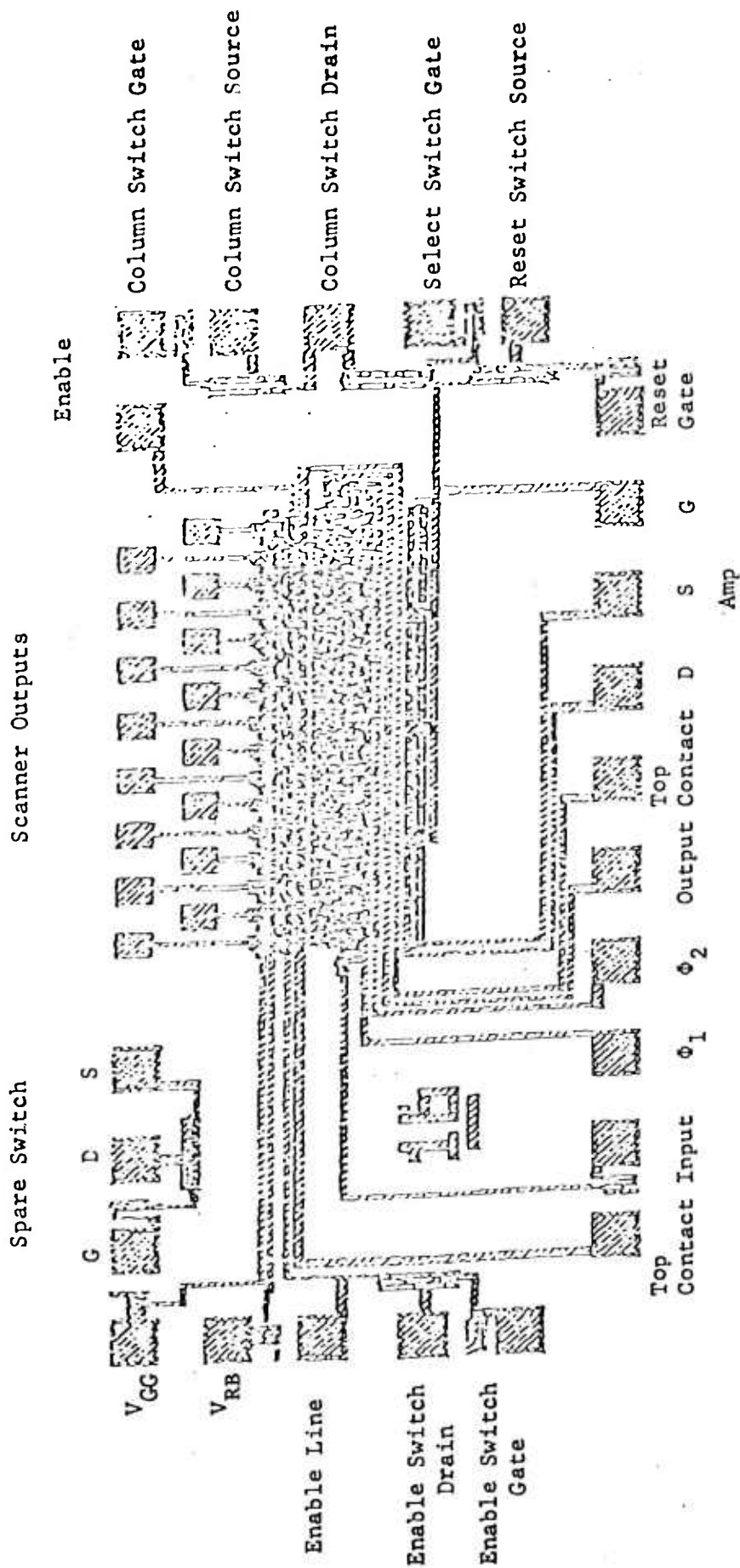


Figure 32. Identification of the Bonding Pads for the Scanner Shown in Figure 31.

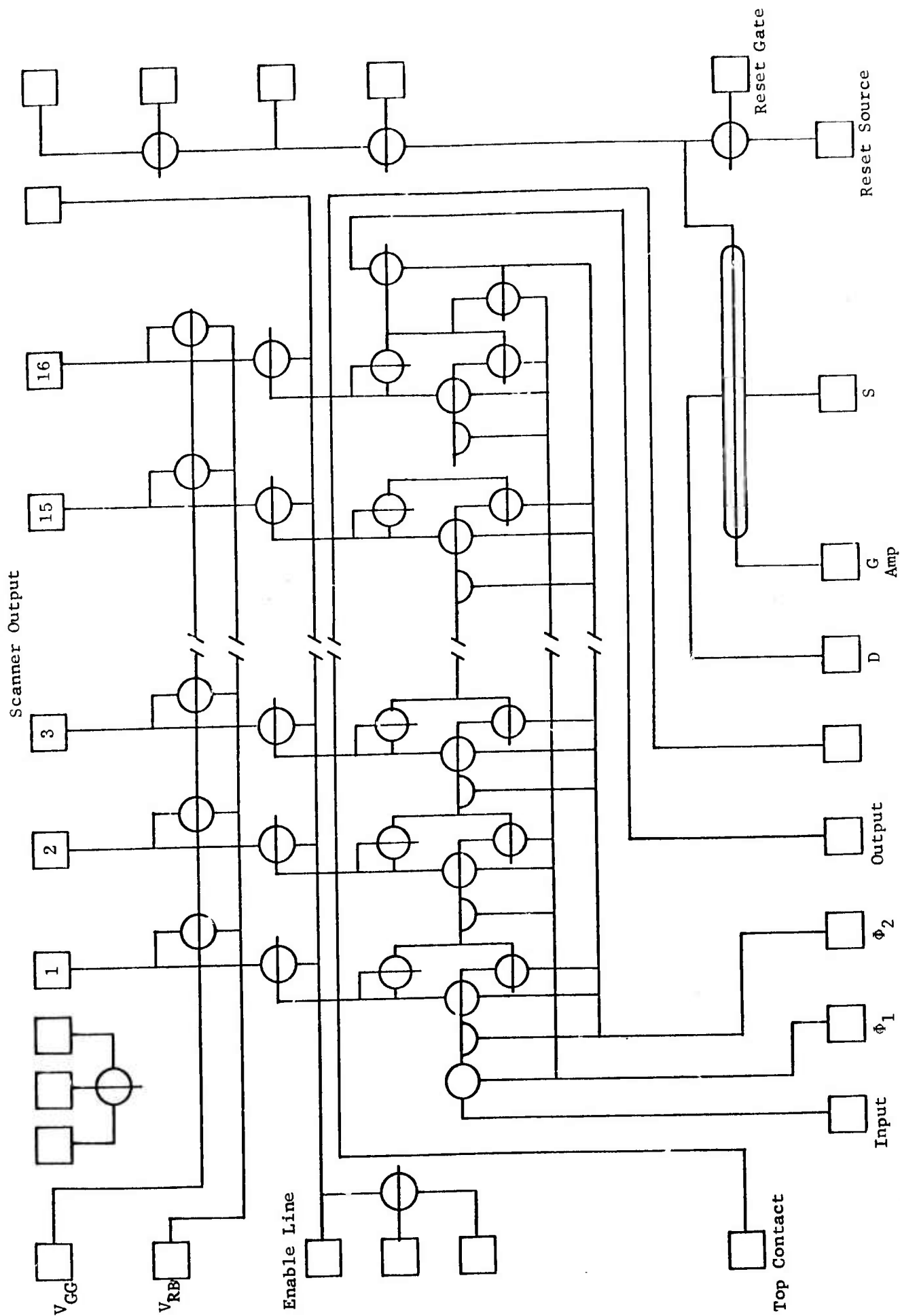


Figure 33. Equivalent Circuit for the Si Scanner Shown in Figure 31.

The scanner output stages were further tested for the actual scanner operation by applying a negative dc voltage source to the enable line with $V_{RB} = 0$. The result of one of the stages (stage No. 1) is shown in Figure 34 the top trace is the input pulse for the scanner and the bottom trace represents the output of stage No. 1. During the negative going pulse time period, the enable switch is turned on, operating the selection function. Thus, these tests indicate that the scanner is properly operated and we then proceed to connect with InSb CID arrays.

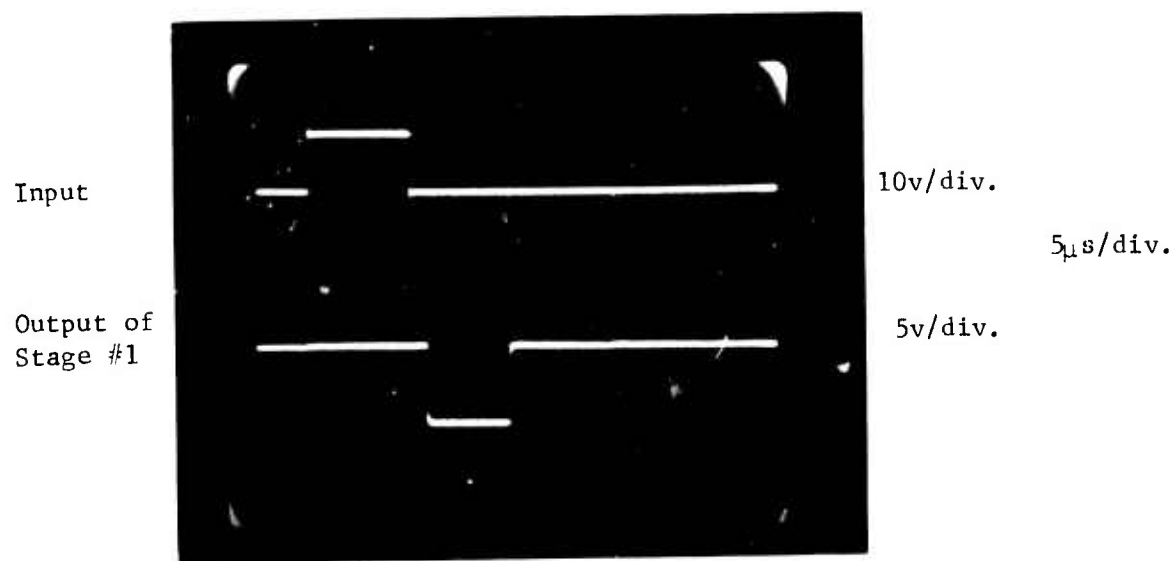


Figure 34. Test Result of the Silicon Scanner Operation

VII. ARRAY EVALUATION AND MEASUREMENTS

1. Measurement Setup

A block diagram of the evaluation system is shown in Figure 35. The InSb array and silicon scanner package were mounted on the cold finger of a cryogenic dewar and operated at the same temperature, approximately 77°K. The MOSFET preamplifier and reset switch were also operated at 77°K in the dewar. The remaining peripheral circuits are located on circuit boards plugged into an appropriate rack conveniently located behind the dewar to minimize connection lead length. These circuits include the timing circuits, bias and drive circuits, sample-and-hold, and post-amplifier circuits.

For easy mounting of the array package in the cryogenic dewar, the special package-mounting fixture illustrated in Figure 3; was designed and built. An Amphenol flatpack socket of 28 lead pins (Part No. 611-10031-281) was incorporated with a specially designed copper cold finger built to fit the demountable dewar. The interconnection leads of low-thermal conductivity wires inside the dewar were soldered to the socket pins according to the array package leads connected to the device. When the array package is mounted in the dewar, it is simply snapped into the flat-pack socket to make contact to the leads; a holding plate and screw is used to hold the package down to the cold finger, as illustrated in Figure 36. This arrangement proved very efficient and saves considerable time. For most array evaluations a filter with a reduced field-of-view aperture was used to minimize the effect of the background photon flux on the array. For dewar electric interconnections, a 27-pin hermetically sealed Deutsch connector (Cat. No. DM5600-27P) was employed.

The optical measurement setup for modulating an image is shown in Figure 37. The common column line of the array was aligned vertically in the dewar and a lens was used to focus a narrow slit (line source) mounted on a central holder. A small wire heater was located behind the slit. The holder can be adjusted for the up and down positions, to move the slit image along the one-column array. That is, as the image moves along the

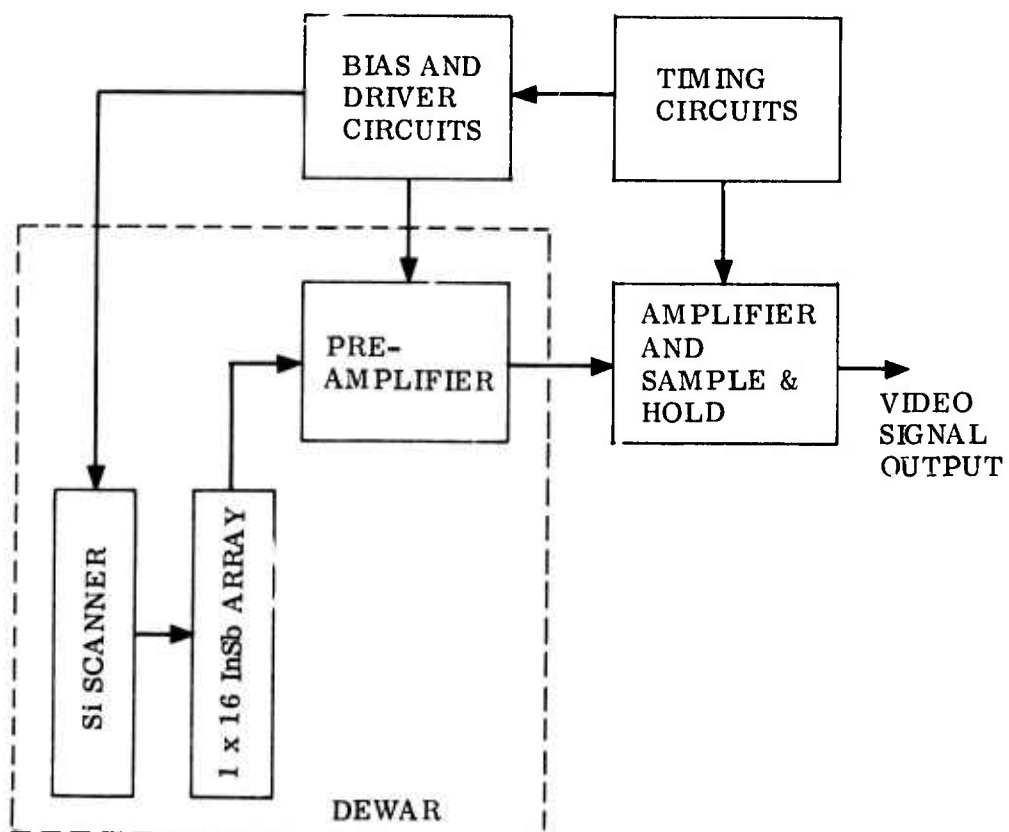


Figure 35. Block Diagram of the Array Testing System.

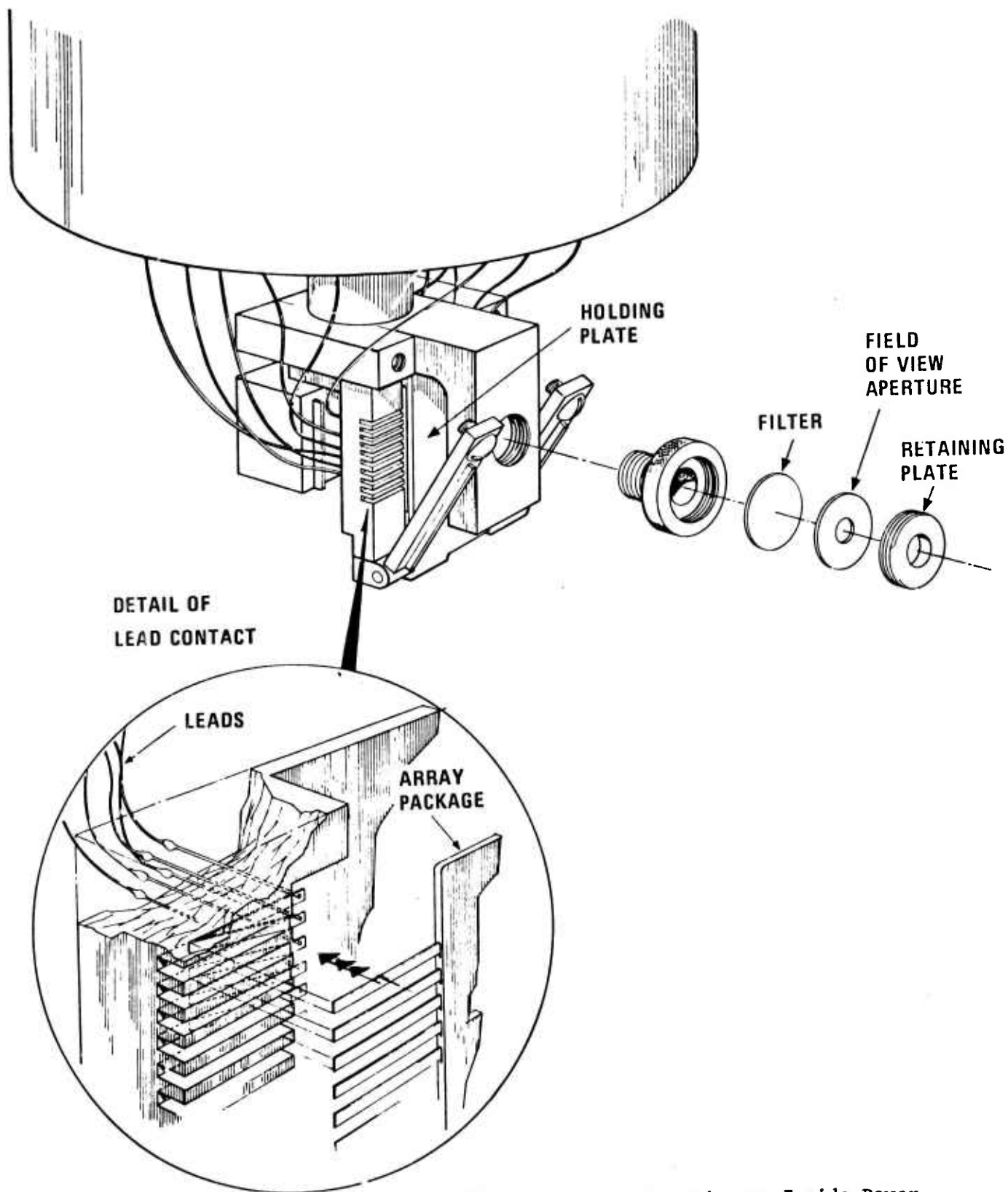


Figure 36. Array Mounting Fixture Inside Dewar

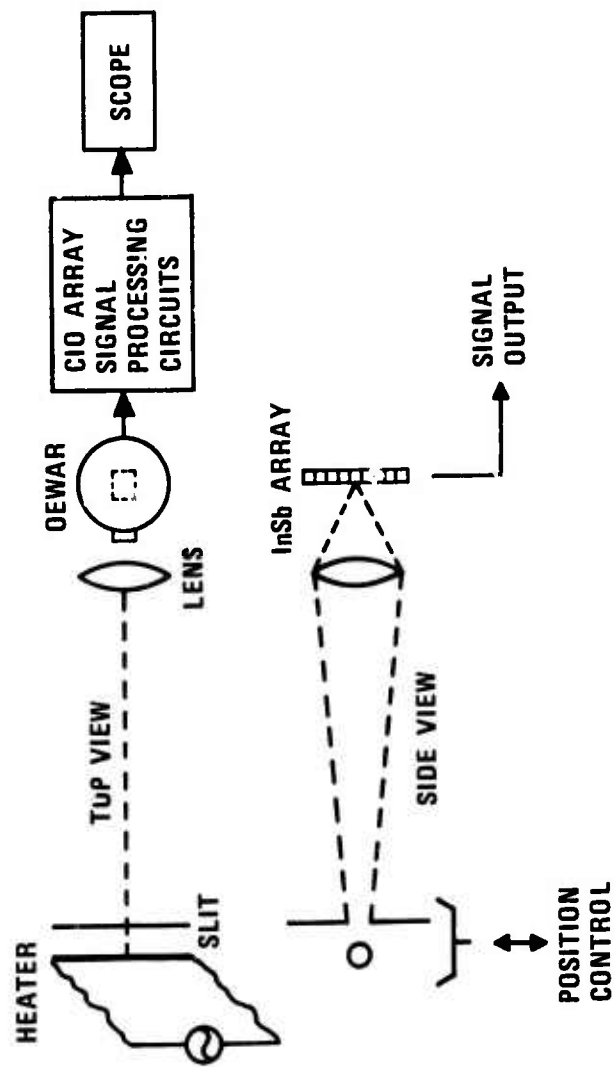


Figure 37. Optical Array Measurement Setup Used for Modulation of a Slit Image.

column line, the 16 row elements should respond. The output signals were then displayed on a scope.

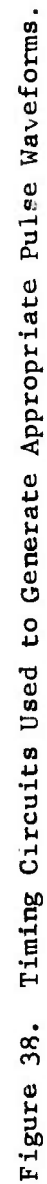
2. Array Test Circuits

The array signal processing circuits are mounted on a rack located behind the dewar on the optical bench. These circuits are divided into three separate circuit boards; timing, bias and driver circuits, and amplifier and sample-and-hold circuits.

a) Timing Circuits

The timing circuits, shown in Figure 38, consist of a master clock, element and line timing circuits, and control flip-flop circuits. CMOS devices are used for the timing circuits. The V_{DD} pin is connected to ground and the V_{SS} pin is connected to -12 volts. Thus, the voltage swing is from ground to -12 volts. The master clock is an RC-oscillator, consisting of two inverters (Z16), two resistors, a capacitor and a potentiometer to adjust the oscillator to the desired frequency. The output of the oscillator serves as the clock pulse for the element timing circuits.

The element timing circuits consist of a 12-bit shift register, decoding gates and control flip-flops. Two Hex D flip-flops (Z_1 and Z_2) are connected as a 12-bit shift register. Decoding gates are connected to the output of the first eleven stages of the shift register and monitor their state. When all of the outputs connected to the decoding gates are "low", a "high" level pulse is generated and applied to the input of the first stage of the shift register. The pulse is shifted through the register; then another pulse is applied to the input when the decoding gate inputs are all "low". This process repeats, serving as the element timing function. Thus, one pulse is shifted through the shift register and is used as a control pulse to generate the Φ_1 , Φ_2 , dc restore, inject, sample, row gate and reset pulses. The output from the second stage of the shift register is used as the clock pulse for the line timing circuits.



The line-timing circuits are similar to the element timing circuits, the only difference being the number of stages and decoding gates. The line-timing circuits consist of three Hex D flip-flops (Z3, Z4 and Z5) connected as an 18-bit shift register. The last two bits of the shift register are used as blanking pulses so that a reference mark is available. Decoding gates connected to the output of the first 17 stages of the shift register monitor their state. When all of the output connected to the decoding gates are "low", a "high" level pulse is applied at the input of the first stage of the shift register. This pulse is shifted through the register and another is applied to the input. The process repeats, serving as the line-timing function. The input pulse is also applied to the silicon scanner, located in the dewar, after inversion and level shifting.

The dc restore, inject, sample, row gate, reset, ϕ_1 , and ϕ_2 pulses are generated by controlling the state of the dual D flip-flops (Z11, Z13, Z14, Z15) with the pulse shifted through the element-timing shift register.

b) Bias and Driver Circuits

The reset, ϕ_1 , ϕ_2 , \overline{SR}_{IN} , row gate, and inject pulses from the timing circuit board are applied to the bias and driver circuit board which is shown in Figure 39. The reset, ϕ_1 , ϕ_2 and row gate pulse are level-shifted from a voltage swing of 0 to -12 volts to 0 to -16 volts. This larger negative voltage is needed for proper scanner operation. The \overline{SR}_{IN} pulse is inverted before it is level-shifted. The inject pulse is inverted and combined with a dc level so that the amplitude of the inject pulse can be varied. The amplitude of the inject pulse, controlled by the injection amplitude adjust potentiometer, can be varied from approximately -1 to -16 volts. The row transfer and row bias voltages are dc, with an amplitude that can be adjusted from 0 to -16 volts. The level of these voltages are controlled by the row transfer and bias amplitude potentiometers. The wipers of the potentiometer are applied to

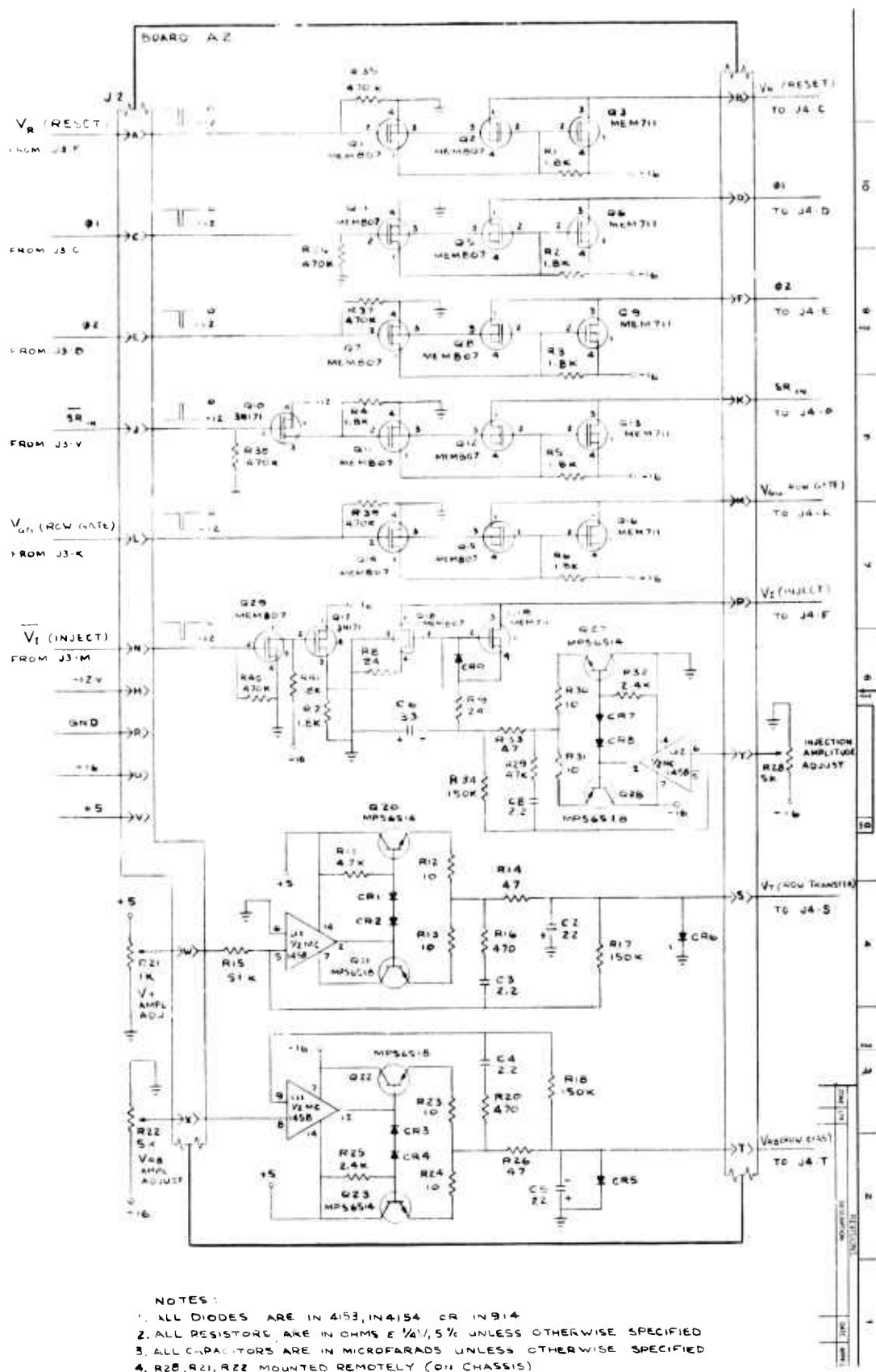


Figure 39. Bias and Driver Circuits.

operational amplifiers. The low impedance output of the amplifiers is also filtered. The timing relationship of these pulses is shown in Figure 40.

c) Amplifier and Sample-and-Hold

The amplifier and sample-and-hold circuits are shown in Figure 41. The inject pulse is ac-coupled to the array through a 5 pF capacitor located in the dewar. A MOSFET transistor is located on the scanner chip in the dewar. The MOSFET has a W/L ratio of 44/.3 and a g_m of 2000 μ mhos at 300°K with a drain current of 2 m amps. The g_m increases to 5000 μ mhos when the temperature of the MOSFET is 77°K.

An operational amplifier connected as an integrator is connected to the source of the MOSFET. A potentiometer, connected to the non-inverting input of the amplifier, is adjusted so that the current through the MOSFET is approximately 2 mA. The video signal is connected to the inverting input of the amplifier. This feedback configuration tends to keep the drain current at approximately 2 mA so that the g_m of the MOSFET is constant. The drain of the MOSFET is connected to the emitter of the common-base transistor, Q1. The MOSFET and Q1, used as a cascode amplifier, exhibits low noise and wide bandwidth characteristics. Also, the common-base configuration of Q1 has a low input impedance, so the transition from the drain of the MOSFET in the dewar to the emitter of Q1 on circuit board A1 by means of a co-axial cable poses no problems.

A resistor, R_1 , connected to the collector of Q1 serves as the load resistor for the cascode configuration. The gain of the cascode stage is approximately 25. The output of the cascode stage is applied to a buffer transistor, Q2, and a clamping circuit, CR2 and CR3, which limits the amplitude of the amplified injection voltage. The emitter of the buffer transistor is applied to the low output impedance driven transistors, Q3 and Q4. The output of these transistors is applied to the integrating amplifier (as described above)

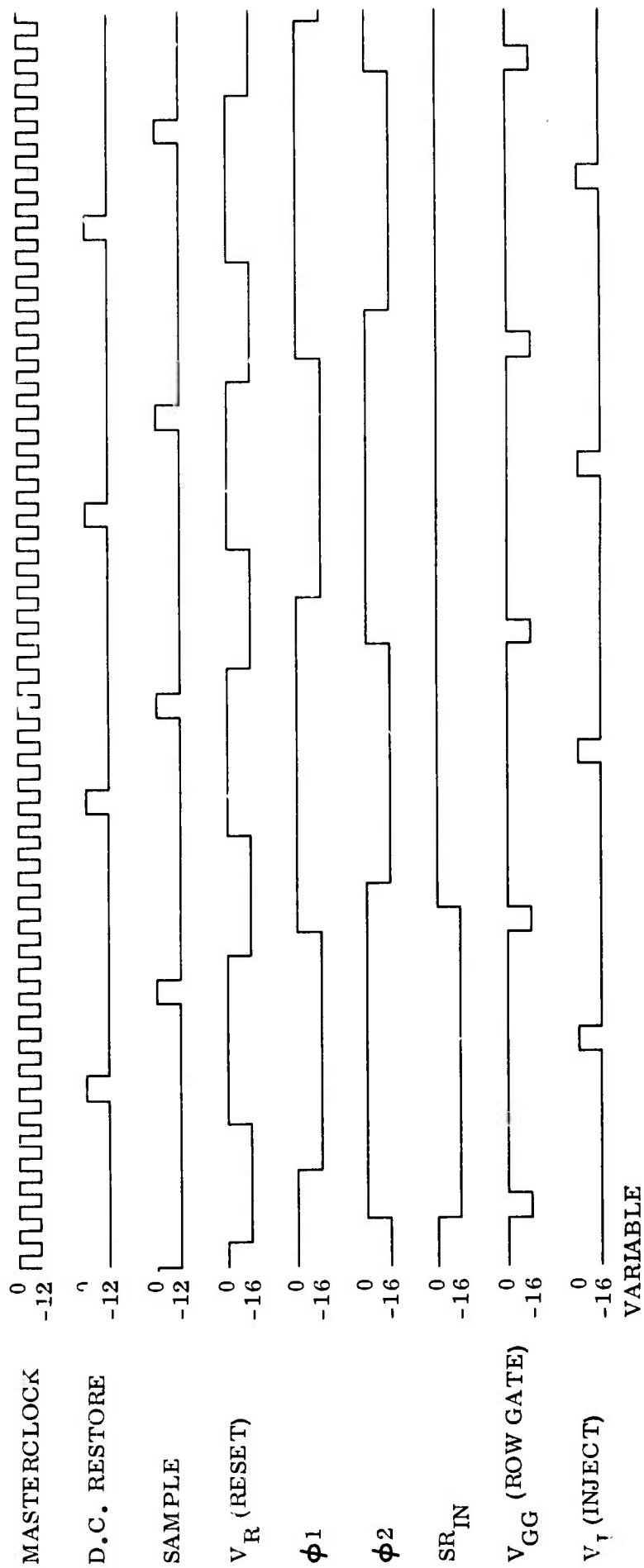


Figure 40. Appropriate Timing Diagram Used for the Array Measurements.

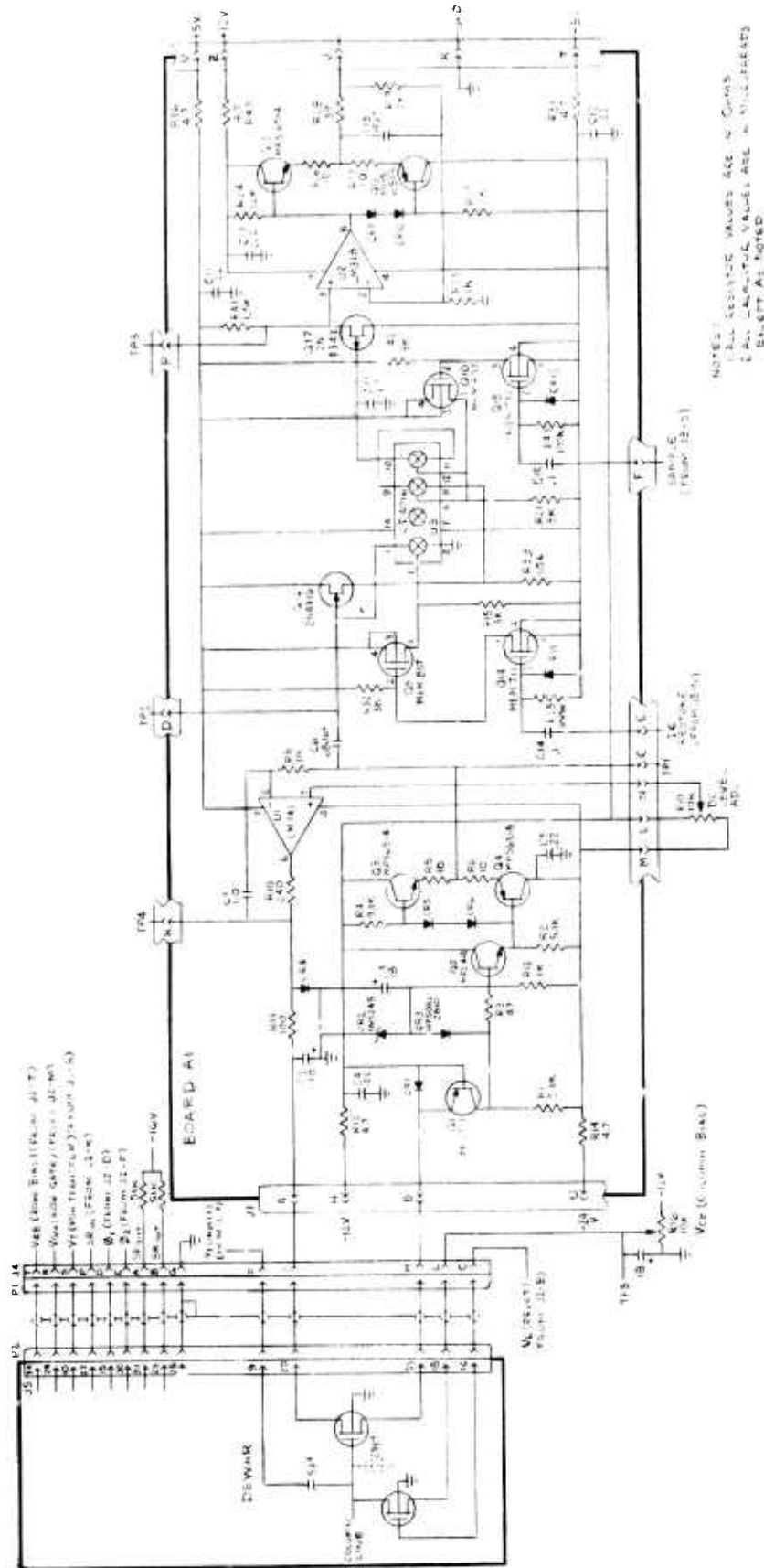


Figure 41. Amplifier and Sample-and-Hold Circuits Used for the Video Signal Processing.

and the dc restore capacitor (C6).

The other side of C6 is connected to the gate of a JFET and the input of a bilateral transmission gate (pin 1 of U3). The dc restore pulse, 0 to -12 volts, is ac-coupled to the gate of Q14. The MOSFETS, Q14 and Q5, level-shift the dc restore pulse to a +5 to -5 volt level so that the control input of the transmission gate is at the proper voltage. When the dc restore pulse is present, the transmission gate turns on and connects one side of the dc restore capacitor (C6) to ground. The dc restore switch eliminates any kTC noise. The source of JFET Q16 is applied to the input of the first of two transmission gates which are connected in series. The output of the second transmission gate is applied to the 2000 pF hold capacitor of the sample-and-hold circuit. When the sample pulse is present, it is level-shifted in the same manner as the dc restore pulse by MOSFETS Q15 and Q10. These MOSFETS control the transmission gates of the sample-and-hold circuit. The two transmission gates in series have a very high resistance when the gates are off, so that the hold capacitor does not lose any of its voltage due to the off resistance of the transmission gates during the hold time. The hold capacitor is connected to the gate of JFET Q17. Q17 is connected as a source follower. The input impedance of the source follower JFET is very large so that there is no loss in voltage across the hold capacitor during the hold time. The output of the source follower, Q17, is applied to the high impedance non-inverting input of the LM318 operational amplifier (U2). U2, Q12, Q13 and associated components form the post-amplifier, which has a gain of three. Thus, the total gain of the amplifiers is approximately 75.

3. Array Measurements

The schematic circuit diagram of an InSb array connected with a silicon shift register scanner and preamplifier is shown in Figure 42. The 16 row elements were connected to the silicon scanners (in this case we used two scanners as indicated previously) and the common column line was

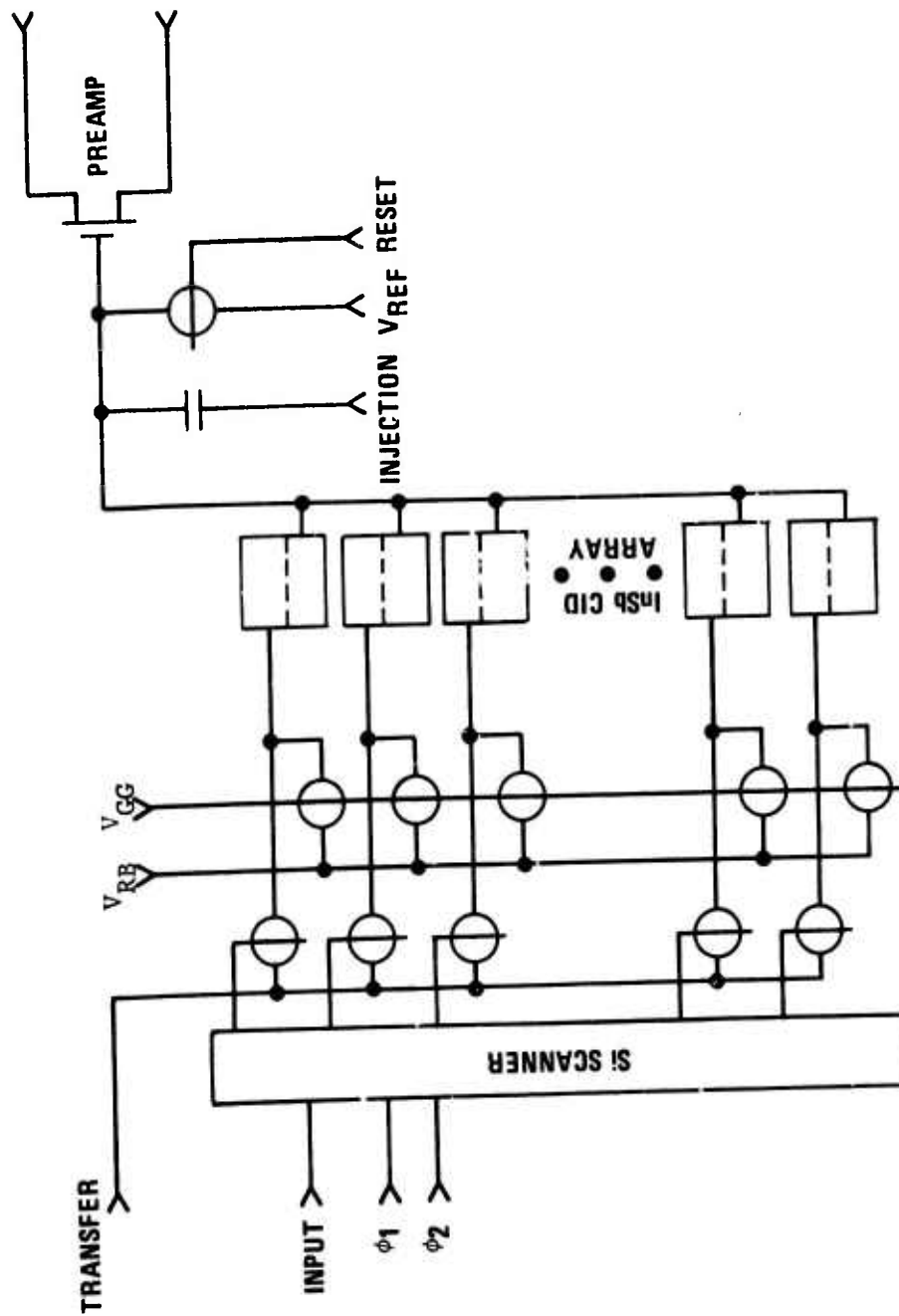


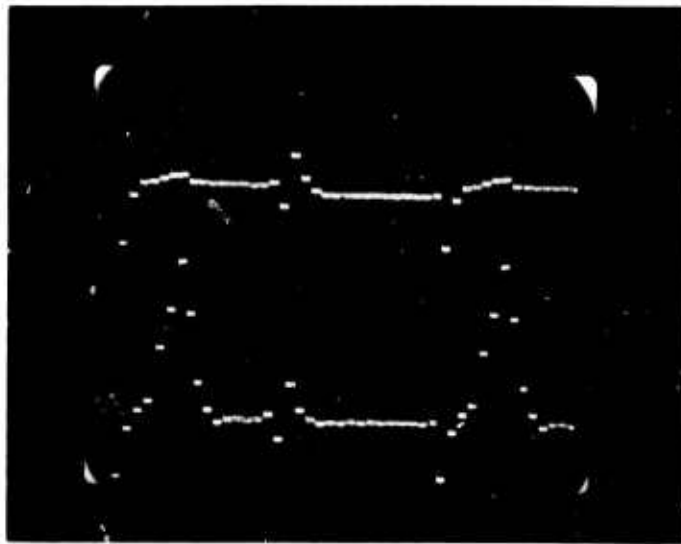
Figure 42. Schematic Diagram of InSb CID Array (1x16) Connected with Si Shift Register Scanner and Preamplifier.

connected to a preamplifier, injection coupling capacitance and a reset switch. The column line is biased with V_{REF} through the reset switch and all of the row gates are biased with V_{RB} through the switches controlled by V_{GG} . These switches are turned on only during the time interval that one enable switch is open and the next enable switch is closed, so that while V_{GG} voltage pulse is applied to the switch gate, none of the enable switches are closed (see Figure 40).

While the row elements are scanned sequentially, the column line is used to read out the signal. When a row element is selected by turning on the enable switch, the charge in the selected row gate must be transferred into the corresponding column electrode. The charge in the selected element can then be read out by charge injection. During this charge injection, however, the charge in all of the unselected column gates must be transferred to the unselected row gates respectively, to avoid the injection. Only charge injection results in a video signal. Therefore, the charge transfer and injection must occur on the basis of element selection; for the selected element, the charge is injected while the charge in unselected elements must be transferred to avoid charge injection.

To demonstrate the two-dimensional mode of operation, an image modulation along the 16-element array was performed with the setup shown in Figure 37. The output video signals are displayed on a scope as shown in Figure 43. The top photo is a single slit image on a more sensitive scale; eight elements respond. The bottom photograph shows three imaged output signals, obtained as the image moves along the array; five elements respond in each image. If the charge were not properly transferred between the row and column gates in each resolution element, no imaged element responses would occur because the common column line is connected to the preamplifier, as shown in Figure 42, and there would be a common signal with no modulation.

Another example of the charge transfer mode of operation is shown in Figure 44. The 16 stages of the silicon scanner (two scanners were used as shown in Figure 26) were driven by the data input, which was applied once every 18 clock pulse intervals, so that no array element was selected during the 17th and 18th clock pulses. During these two clock pulse intervals,



With No Image

With a Line Image

Scale: $V = 0.5 \text{ volt/div.}$

$H = 0.1 \text{ msec/div.}$



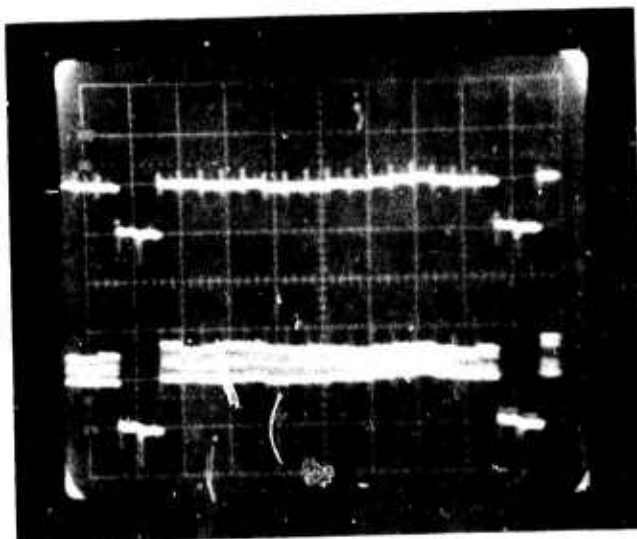
As a Line Image Moves
Along the Array

Scale: $V = 1.0 \text{ volt/div.}$

$H = 0.1 \text{ msec/div.}$

Figure 43. Array, Demonstrating Two-Dimensional
Mode of Operation.

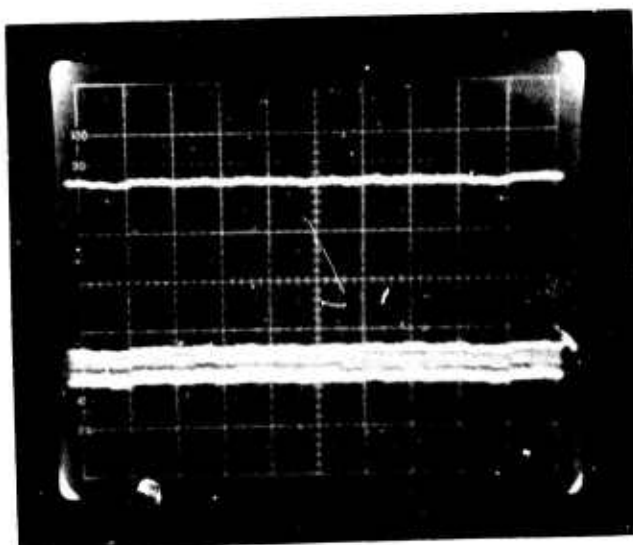
**CHARGE
TRANSFER
MODE**



**WITHOUT
SIGNAL**

**WITH
SIGNAL**

**SINGLE
COLUMN
CELL
OPERATION
(ALL
ROW CELLS
ARE
GROUNDED)**



**WITHOUT
SIGNAL**

**WITH
SIGNAL**

**SCALE: V = 0.5 V/DIV
H = 50 μ s/DIV**

Figure 44. Operation of 1x16 Array Using a Blackbody Source

therefore, there is no output signal, as shown in the top photo of Figure 44, indicating that charge transfer takes place. In this experiment, a blackbody source was irradiated uniformly on the array and a chopper was used to modulate the signal. The multi-lines represent the modulated signal. As shown, during the 17th and 18th clock pulse intervals, there is no modulated signal present, indicating that the array is operating in the two-dimensional mode. This is further illustrated in the lower photograph. When all the row electrodes are grounded, the column line operates as a single element structure. Therefore, there is a signal present during every clock pulse period, as shown in the lower photograph of Figure 44. In this case, no charge transfer occurs, thus an output signal is produced for every clock pulse, lending further support that the array is operating properly.

VIII. CONCLUSIONS AND RECOMMENDATIONS

Two-dimensional InSb CID arrays have been successfully fabricated and operated. The relevant interface properties of the InSb MIS structures are related directly to the fabrication technology and have been improved considerably. A considerable improvement in the interface state density has been obtained and surface state densities as low as mid- $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ have been realized. High vacuum annealing produces a low surface state density, but the mechanism by which this improvement results has not been determined. The result is particularly important for IR devices, since these devices are eventually packaged in vacuum dewars, which are normally baked out in high vacuum before being sealed off. During these bakeouts, the IR devices must not be degraded.

The InSb CID linear arrays yield high-sensitivity; all the noise sources in these devices have been identified and the measured results compared favorably with theoretical values. For background photon flux levels higher than mid- $10^{12} \text{ photons/sec-cm}^2$ range, device performance is practically background limited (BLIP). The measured values of noise-equivalent carriers are equal to the shot noise of the background generated carriers and are proportional to the square root of the carriers generated by the background photon flux. In the lower background region at 77°K , however, the amplifier and shot noise associated with the thermally generated dark current basically limits the sensitivity of the device. The lowest measured number of noise-equivalent carriers is about 200, with a background photon flux density of $10^{12} \text{ photons/sec-cm}^2$; the theoretical noise value for this background level is about 120 carriers. The additional noise values are due to the amplifier (100 carriers) and the dark current (140 carriers).

InSb CID, 1×16 one-column, two-dimensional arrays have been fabricated using the InSb MIS technology. Due to the two-dimensional structure, a multi-layer metallization process must be used; 17 processing steps are needed to complete the array, requiring nine mask sets. The charge transfer between the row and column gates in each resolution element, which is

required for two-dimensional array operation, has been accomplished using an overlapped gate configuration.

Based on these results, we recommend that this program be extended to the development of 16x25 area arrays for use in the series-parallel scan IR focal plane.

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